Customer Care Solutions
NHL-4J/NHL-4JX Series Transceivers

System Module and User Interface

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Glossary of Terms

ACI	Accessory Control Interface
ADC	Analog-Digital Converter
AEC	Acoustic Echo Canceller
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
AIF	Application Interface
ALWE	Background noise suppressor
AMS	After Market Service
API	Application Programming Interface
ARM	Processor architecture
ASIC	Application Specific Integrated Circuit
BB	Baseband
BT	Bluetooth
CBus	Control Bus connecting UPP_WD2 with UEM
CCI	Camera Control Interface
CCP	Compact Camera Port
CMT	Cellular Mobile Telephone (MCU and DSP)
CPU	Central Processing Unit
CTSI	Clocking Timing Sleep Interrupt
COBBA_GJP	DCT3 RF-interface and audio codec ASIC with serial MAD interface
COG	Chip On Glass
CSP	Chip Scale Package
CSTN	Color Super Twisted Nematic
DAC	Digital-Analog Converter

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DAI	Digital Audio Interface
DB	Dual band
DCS1800	Digital Cellular system at 1800 MHz
DCT3	Digital Core Technology, 3rd generation
DCN	Offset Cancellation control signal
DLL	Dynamic Link Library
DRC	Dynamic Range Controller
DSP	Digital Signal Processor
EGSM	Extended – GSM
EFR	Enhanced Full Rate
EGPRS	Enhanced General Packet Radio Service
EMC	Electromagnetic compatibility
EMI	Electromagnetic Interference
ESD	Electro Static Discharge
EXT RF	External RF
FBUS	Asynchronous Full Duplex Serial Bus
GPRS	General Packet Radio Service
GSM	Global System for Mobile communications
HS	Half Rate Speech
HSCSD	High Speed Circuit Switched Data
IC	Integrated Circuit
HF	Integrated Hands Free
I/O	Input/Output
IrDA	Infrared Association

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LCD	Liquid Crystal Display
LDO	Low Drop-Out
LNA	Low Noise Amplifier
MBUS	1-wire half duplex serial bus
MCU	Micro Controller Unit
MDI	MCU-DSP Interface
MFI	Modulator and Filter Interface
PA	Transmit Power Amplifier
PC	Personal Computer
PCM	Pulse Code Modulation
PCM SIO	Synchronous serial bus for PCM audio transferring
PIFA	Planar Inverted F-antenna
PWB	Printed Wiring Board
RF	Radio Frequency
SIM	Subscriber Identity Module
UEM	Universal Energy Management
UI	User Interface
UPP	Universal Phone Processor
VCXO	Voltage Controlled Crystal Oscillator
VCTCXO	Voltage Controlled Temperature Compensated Crystal Oscillator.

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Introduction

Electrical Modules

The system module TB3 consists of Radio Frequency (RF) and baseband (BB). User Interface (UI) contains display, keyboard, IR link, vibra, HF/HS connector and audio parts.

FM radio is located on the main PWB TB3.

The electrical part of the keyboard is located in separate UI PWB named TK8. TK8 is connected to radio PWB through spring connectors.

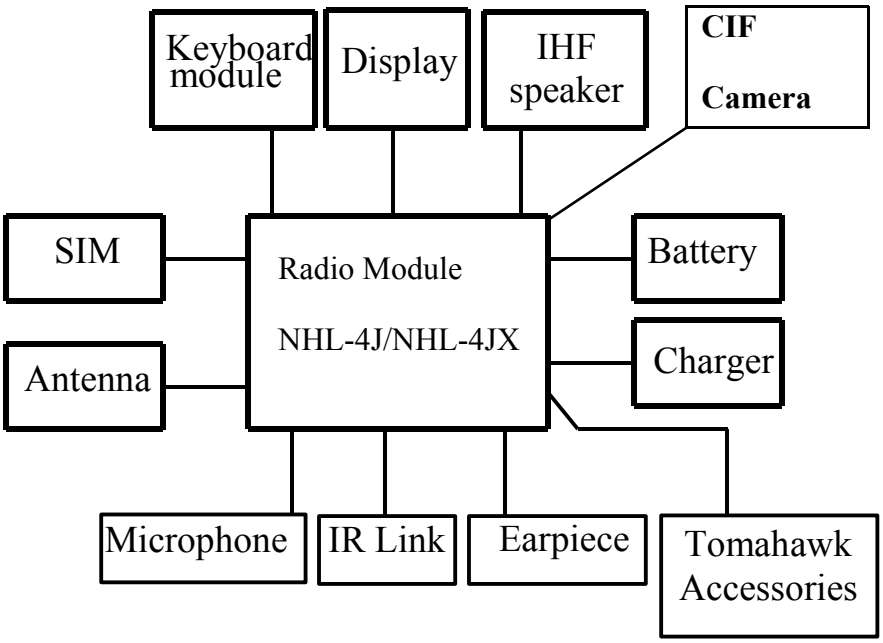
The Baseband blocks provide the MCU, DSP, external memory interface and digital control functions in the UPP ASIC. Power supply circuitry, charging, audio processing and RF control hard ware are in the UEM ASIC.

The purpose of the RF block is to receive and demodulate the radio frequency signal from the base station and to transmit a modulated RF signal to the base station.

The UI module is described in this section of the manual.

Interconnection Diagram

Figure 1: Interconnection diagram



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Temperature Conditions

Specifications are met within range of -10...+55 deg. C ambient temperature
Storage temperature range -40...+70 deg. C

Humidity

Relative humidity range is 5... 95%.
This module is not protected against water. Condensated or splashed water might cause malfunction momentary. Long term wetness will cause permanent damage.

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System Module : Baseband

The System module (or Engine) consists of Baseband and RF sub-modules, each described below.

Baseband Module, technical summary

Main functionality of the baseband is implemented into two ASICs: UPP (Universal Phone Processor) and UEM (Universal Energy Management).

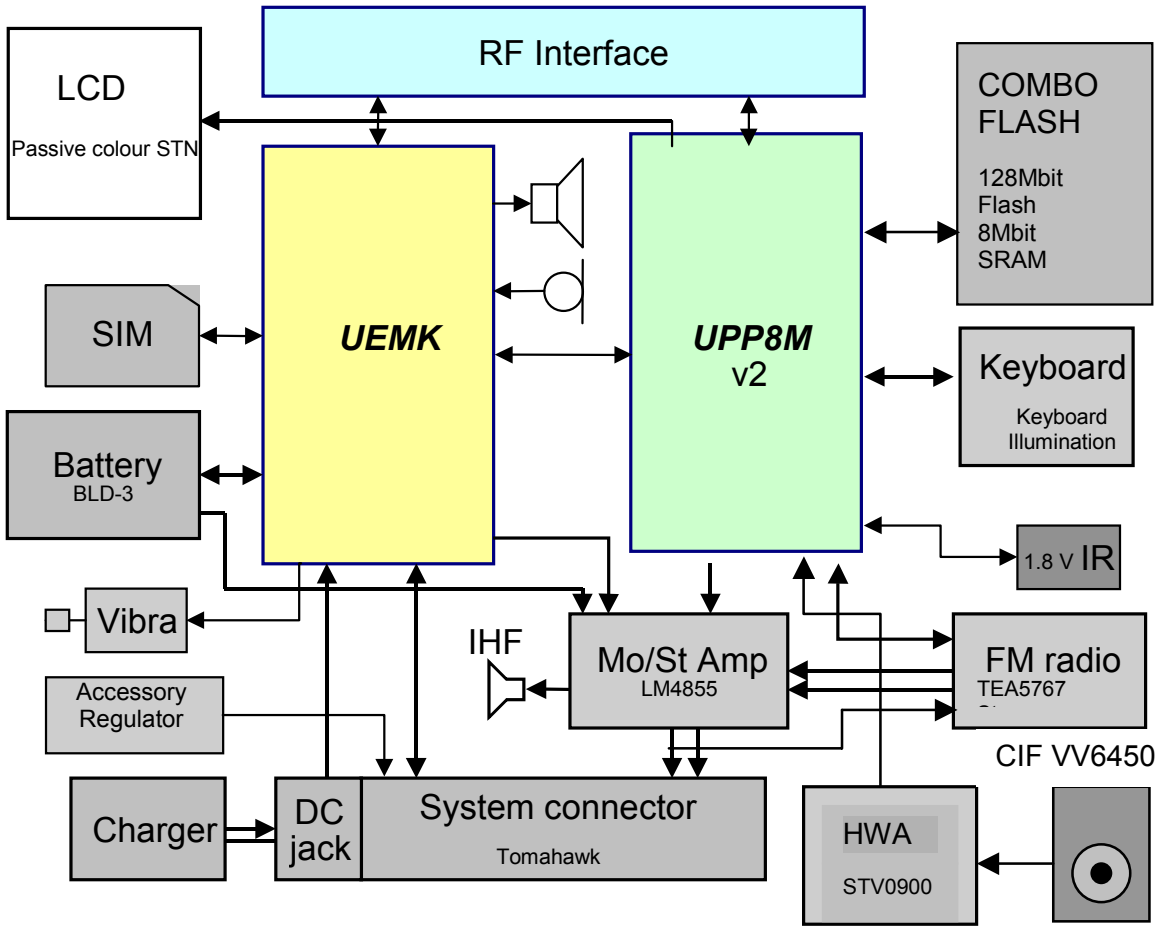

Figure 2: Baseband block diagram

Baseband is running from power rails 2.8V analog voltage and 1.8V I/O voltage. UPP core voltages can be lowered down to 1.0V, 1.3V and 1.5V. UEM includes 6 linear LDO (Low Drop-Out) regulator for baseband and 7 regulators for RF. It also includes 4 current sources for biasing purposes and internal usage. UEM also includes SIM interface which has supports both 1.8V and 3V SIM cards. **Note:** 5V SIM cards are no longer supported by DCT-4 generation baseband.

A real time clock function is integrated into the UEM, which utilizes the same 32kHz clock supply as the sleep clock. A backup power supply is provided for the RTC-battery, which keeps the real time clock running when the main battery is removed. The backup power supply is a rechargeable surface mounted Li-Ion battery. The backup time with the battery is 30 minutes minimum.

A UEM ASIC handles the analog interface between the baseband and the RF section.

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UEM provides A/D and D/A conversion of the in-phase and quadrature receive and transmit signal paths and also A/D and D/A conversions of received and transmitted audio signals to and from the user interface. The UEM supplies the analog TXC and AFC signals to RF section according to the UPP DSP digital control. Data transmission between the UEM

Technical Summary

Baseband of the NHL-4J/NHL-4JX is running from power rails 2.8V analog voltage and 1.8V I/O voltage. UPP core voltages can be lowered down to 1.0V, 1.3V and 1.5V. UEM includes 6 linear LDO regulators for baseband and 7 regulators for RF. It also includes 4 current sources for biasing purposes and internal usage. UEM also includes SIM interface which has supports both 1.8V and 3V SIM cards.

A real time clock function is integrated into the UEM, which utilizes the same 32kHz clock supply as the sleep clock. A backup power supply is provided for the RTC-battery, which keeps the real time clock running when the main battery is removed. The backup power supply is a rechargeable surface mounted Li-Ion battery. The backup time with the battery is 30 minutes minimum.

A UEM ASIC handles the analog interface between the baseband and the RF section**.** UEM provides A/D and D/A conversion of the in-phase and quadrature receive and transmit signal paths and also A/D and D/A conversions of received and transmitted audio signals to and from the user interface. The UEM supplies the analog TXC and AFC signals to RF section according to the UPP DSP digital control. Data transmission between the UEM and the UPP is implemented using two serial busses, DBUS for DSP and CBUS for MCU. There are also separate signals for PCM coded audio. Digital speech processing is handled by the DSP inside UPP ASIC. UEM is a dual voltage circuit, the digital parts are running from the baseband supply 1.8V and the analog parts are running from the analog supply 2.78V. Also VBAT is directly used (Vibra, LED-driver, Audio amplifier).

The baseband supports both internal and external microphone inputs and speaker outputs. Input and output signal source selection and gain control is performed by the UEM according to control messages from the UPP. Keypad tones, DTMF, and other audio tones are generated and encoded by the UPP and transmitted to the UEM for decoding. An external vibra alert control signals are generated by the UEM with separate PWM outputs.

NHL-4J/NHL-4JX has two serial control interfaces: FBUS and MBUS. FBUS can be accessed through a test pad and the System Connector as described later. The MBUS can be accessed through the test pads as described in section MBUS Interface

EMC shielding is implemented using a metallized plastic frame. On the other side, the engine is shielded with PWB grounding.

Environmental Specifications

Temperature Conditions

Full functionality through ambient temperature range -10 ^{o}C to +55 ^{o}C.

Reduced functionality between -25 ^{o}C to -10 ^{o}C and +55 ^{o}C to +75 ^{o}C.

Humidity and Water Resistance

Full functionality in humidity range is 5% - 95%.

Condensed or dripping water may cause intermittent malfunctions. Protection against dripping water is implemented.

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Baseband Technical Specifications

Absolute Maximum Ratings

Signal	Note
Battery Voltage (Idle)	-0.3V - 5.5V
Battery Voltage (Call)	Max 4.8V
Charger Input Voltage	-0.3V - 16V

DC Characteristics

Regulators and Supply Voltage Ranges

Battery Voltage Range

Signal	Min.	Nom	Max	Note
VBAT	3.1V	3.6V	4.2V (charging high limit voltage)	3.1V SW cut off

Camera Regulator

Vout/ V (min)	Vout/ V (typ)	Vout/ V (max)	Notes
1.728	1.80	1.872	Imax=150mA

BB Regulators

Signal	Min.	Nom	Max	Note
VANA	2.70V	2.78V	2.86V	I_{max} = 80mA
VFLASH1	2.70V	2.78V	2.86V	I_{max} = 70mA I_{sleep} = 1.5mA
VFLASH2	2.70V	2.78V	2.86V	I_{max} = 40mA
VSIM	1.745V 2.91V	1.8V 3.0V	1.855V 3.09V	I_{max} = 25mA I_{sleep} = 0.5mA
VIO	1.72V	1.8V	1.88V	I_{max} = 150mA I_{sleep} = 0.5mA
VCORE	1.0V 1.235V 1.425V 1.710V	1.053V 1.3V 1.5V 1.8V	1.106V 1.365V 1.575V 1.890V	I_{max} = 200mA I_{sleep} = 0.2mA Default value 1.5V

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Accessory Regulator

Signal	Min	Nom	Max	Note
Vout	2.72V	2.80	2.88V	I_{max} = 70mA

RF Regulators

Signal	Min	Nom	Max	Note
VR1A	4.6V	4.75V	4.9V	I_{max} = 10mA
VR2	2.70V 3.20V	2.78V 3.3V	2.86V 3.40V	I_{max} = 100mA
VR3	2.70V	2.78V	2.86V	I_{max} = 20mA
VR4	2.70V	2.78V	2.86V	I_{max} = 50mA I_{sleep} = 0.1mA
VR5	2.70V	2.78V	2.86V	I_{max} = 50mA I_{sleep} = 0.1mA
VR6	2.70V	2.78V	2.86V	I_{max} = 50mA I_{sleep} = 0.1mA
VR7	2.70V	2.78V	2.86V	I_{max} = 45mA

Current Sources

Signal	Min	Nom	Max	Note
IPA1 and IPA2		0mA - 5mA		Programmable, +/-6% V_{IPA1},V_{IPA1} = 0V - 2.7V
IPA3 and IPA4	50µA	100µA	105µA	V_{IPA1} = 0V - 2.7V

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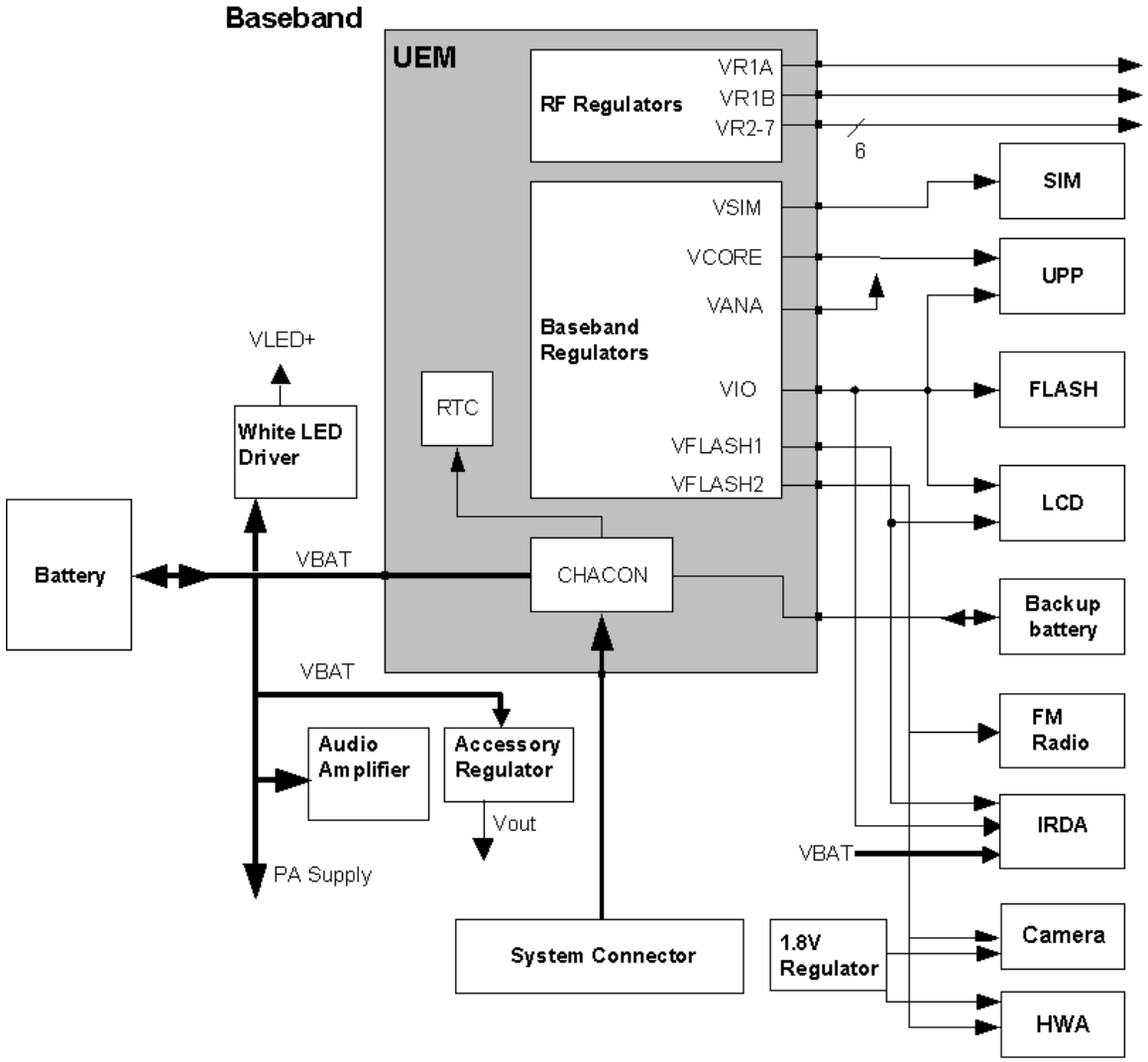
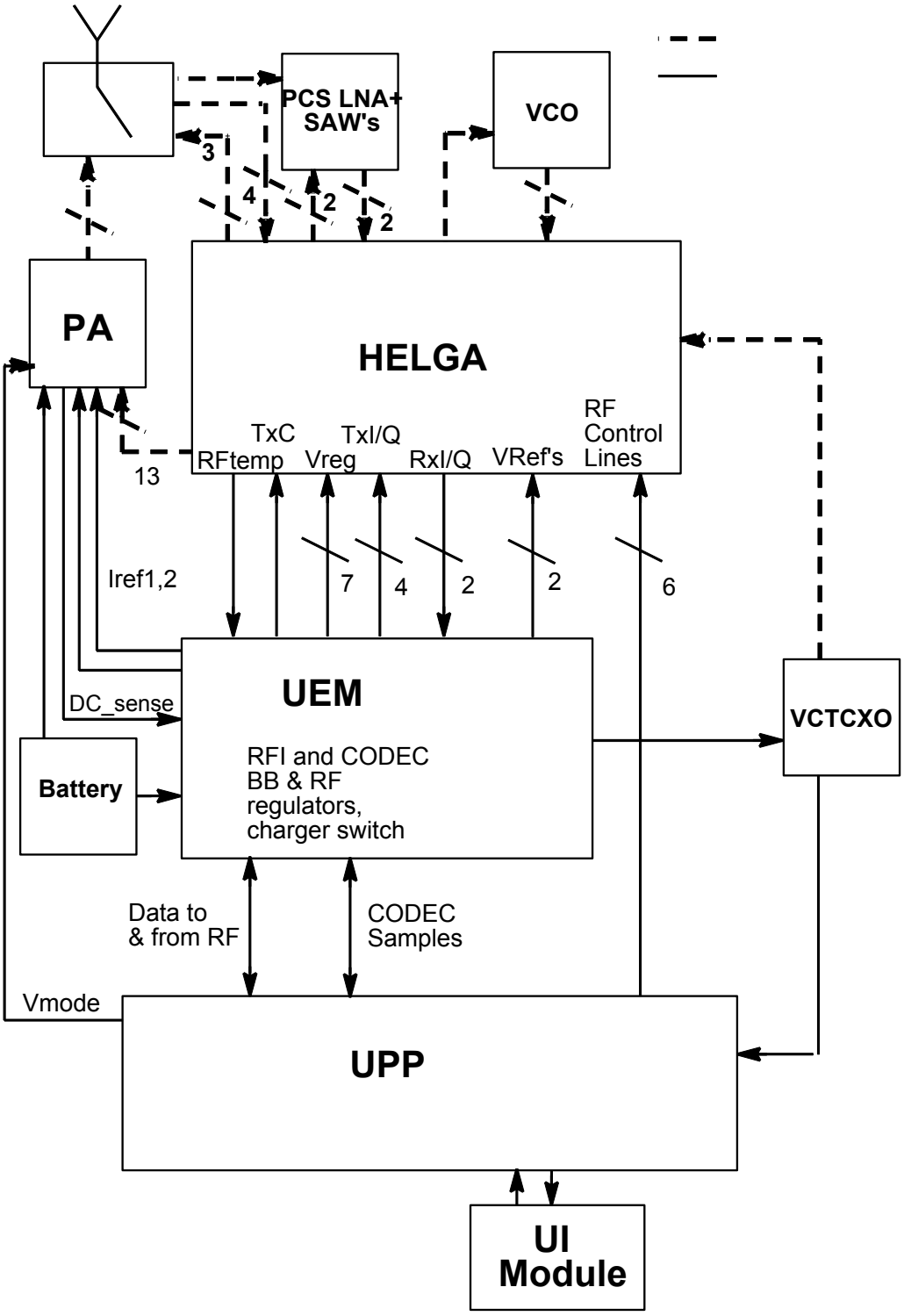
Power Distribution diagram



Baseband External and Internal Signals and Connections

This section describes the external and internal electrical connection and interface levels on the baseband. The electrical interface specifications are collected into tables that cover a connector or a defined interface.

Figure 3: RF/BB connections block diagram



Camera interface

Table 1: Power supply characteristics

Signal name	Type	Min	Typical	Max	Unit	Description
VIO	IN	1.7	1.8	1.9	V	Digital supply
VANA	IN	2.7	2.78	2.9	V	Analogue supply
GND			0		V	System GND

Table 2: DC characteristics

Signal name	Type	Min	Typical	Max	Unit	Description
CSX	IN	H: 0.7xVIO L: 0		H: VIO L: 0.3xVIO	V	Camera chip-select (active low)
DaClk	IN	H: 0.7xVIO L: 0		H: VIO L: 0.3xVIO	V	Voltage levels
TxDa	OUT	H: 0.8xVIO L: 0		H: VIO L: 0.2xVIO	V	Data to transmit, camera interrupt (active low)
RxDa	IN	H: 0.7xVIO L: 0		H: VIO L: 0.3xVIO	V	Data to receive
ExtClk	IN	0.5Vp-p	1Vp-p	VIOp-p	V	All modes
VCtrl	IN	H: 0.7xVIO L: 0		H: VIO L: 0.3xVIO	V	Logic 0: shutdown.

Note: H stands for high signal level and L for low signal level.

Table 3: AC Characteristics

Signal name	Type	Min	Typ	Max	Unit	Description
DaCLK	IN	0	-	8.8[1]	MHz	Frequency
		45/55	50/50	55/45	%	Duty cycle
ExtClk	IN	12.9	13.0	13.1	MHz	External system clock (mode 4)

Note 1: However, DaClk frequency will not exceed ExtClk/2.

Integrated HF Speaker

Signal	Min	Nom	Max	Condition	Note
IHFP	0.75V	0.8V	2.0 V_{pp} 0.85V	AC DC	Differential output (V_{diff} = 4.0 V_{pp})
IHFN	0.75V	0.8V	2.0 V_{pp} 0.85V	AC DC	

FM Radio Interface

BB Signal	FM Radio Signal	Min	Nom	Max	Condition	Note
VFLASH2	Vcca	2.7V	2.78V	2.86V		I_{max} =10.5 mA
	Vcc(vco)	2.7V	2.78V	2.86V		I_{max} =940 µA
	Vccd	2.7V	2.78V	2.86V		I_{max} = 3.9 mA
GenIO(3)	FMClk	1.4V 0	1.8V	1.88V 0.4V	High Low	Reference clock for FM radio module
			32kHz		Frequency	Also 6.5 MHz can be used
		30ppm			Stability	
GenIO(8)	FMWrEn	1.4V 0V	1.8V	1.88V 0.4V	High Low	Write/Read enable
GenIO(12)	FMCtrlDa	1.4V 0	1.8V	1.88V 0.6V	High Low	Bi-directional data
GenIO(11)	FMCtrlClk	1.4V 0	1.8V	1.88V 0.6V	High Low	
				1 MHz	Frequency	
FM Antenna	RFI1, RFI2	76 MHz		108 MHz		FM Input frequency
FM Radio L FM Radio R	VAFL VAFR		100mV			Audio level
		24 dB	30 dB		Channel separation	
		54dB	60 dB		(S+N)/N	
				2%	Harmonic distortion	

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Internal Speaker

Signal	Min	Nom	Max	Condition	Note
EARP	0.75V	0.8V	2.0 V_{pp} 0.85V	AC DC	Differential output (V_{diff} = 4.0 V_{pp})
EARN	0.75V	0.8V	2.0 V_{pp} 0.85V	AC DC	

Integrated HF Speaker

Signal	Min	Nom	Max	Condition	Note
IHFP	0.75V	0.8V	2.0 V_{pp} 0.85V	AC DC	Differential output (V_{diff} = 4.0 V_{pp})
IHFN	0.75V	0.8V	2.0 V_{pp} 0.85V	AC DC	

AC and DC Characteristics of RF-Baseband Voltage Supplies

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Function
VBAT	Battery	PA, UEM	Voltage	2.95	3.6	4.2	V	Battery supply. Cut-off level of DCT4 regulators is 3.04V. Losses in PWB tracks and ferrites are taken account to minimum battery voltage level.
			Current			2000	mA	
			Current drawn by PA when "off"		0.8	2	µA	
VR1A	UEM	HELGA	Voltage	4.6	4.75	4.9	V	Supply for charge pump for SHF VCO tuning.
			Current		2	10	mA	
VR2	UEM	HELGA	Voltage	2.70	2.78	2.86	V	Supply for I/Q-modulators, buffers, ALS
			Current		65	100	mA	
VR3	UEM	VCTCXO, HELGA	Voltage	2.70	2.78	2.86	V	Supply for VCTCXO, PLL digital parts
			Current		1	20	mA	
VR4	UEM	HELGA	Voltage	2.70	2.78	2.86	V	Supply for Helga RX; PA bias blocks.
			Current			50	mA	

VR5	UEM	HELGA	Voltage	2.70	2.78	2.86	V	Supply for Helga PLL; dividers, LO- buffers, prescaler,
			Current			50	mA	
VR6	UEM	HELGA	Voltage	2.70	2.78	2.86	V	Supply for Helga BB and LNAs
			Current			50	mA	
VR7	UEM	SHF VCO	Voltage	2.70	2.78	2.86	V	Supply for SHF VCO
			Current			30	mA	
VrefRF01	UEM	HELGA	Voltage	1.334	1.35	1.366	V	Voltage Reference for HELGA DCN2 op.amps.
			Current			100	µA	
VrefRF02	UEM	VB_EXT	Voltage	1.334	1.35	1.366	V	Voltage reference for HELGA bias block.
			Current			100	µA	
			Temp Coefficient	-65		+65	µV/C	

AC and DC Characteristics of RF-Baseband Digital Signals

Signal name	From	To	Parameter	Input Characteristics				Function
				Min	Typ	Max	Unit	
TXP (RFGenOut3)	UPP	HELGA	"1"	1.38		1.88	V	Power amplifier enable
			"0"	0		0.4	V	
			Load Resistance	10		220	kΩ	
			Load Capacitance			20	pF	
			Timing Accuracy			1/4	symbol	
TXA	UPP	HELGA	"1"	1.38		1.88	V	Power control loop enable
			"0"	0		0.4	V	
			Load Resistance	10		220	kΩ	
			Load Capacitance			20	pF	
			Timing Accuracy			1/4	symbol	
RFBusEna1X	UPP	HELGA	"1"	1.38		1.88	V	RFbus enable

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			"0"	0		0.4	V	
			Current			50	µA	
			Load resistance	10		220	kΩ	
			Load capacitance			20	pF	
RFBusData	UPP	HELGA	"1"	1.38		1.88	V	RFbus data; read/ write
			"0"	0		0.4	V	
			Load resistance	10		220	kΩ	
			Load capacitance			20	pF	
			Data frequency			10	MHz	
RFBusClk	UPP	HELGA	"1"	1.38		1.88	V	RFBus clock
			"0"	0		0.4	V	
			Load resistance	10		220	kΩ	
			Load capacitance			20	pF	
			Data frequency			10	MHz	
Mode Select (GENIO9)	UPP	HELGA	"1"	1.38		1.85	V	Band Selection
			"0"	0		0.4	V	
RESET (GENIO6)	UPP	HELGA	"1"	1.38		1.85	V	Reset to Helga
			"0"	0		0.4	V	
			Load capacitance			20	pF	
			Load resistance	10		220	kΩ	
			Timing accuracy			1/4	symbol	

AC and DC Characteristics of RF-Baseband Analogue Signals

Signal name	From	To	Parameter	Min	Typ	Max	Unit	Function
VCTCXO	VCTCXO	UPP	Frequency	13		26	MHz	High stability clock signal for the logic circuits, AC coupled. Distorted sine-wave e.g. sawtooth.
			Signal amplitude	0.2	0.8	2.0	Vpp	
			Input Impedance	10			kΩ	

			Input Capacitance			10	pF	
			Duty Cycle	40		60	%	
VCTCXOGnd	VCTCXO	UPP	DC Level		0		V	Ground for reference clock
RXI/RXQ	HELGA	UEM	Voltage swing (static)	1.35	1.4	1.45	Vpp	Received demodulated IQ signals
			DC level	1.3	1.35	1.4	V	
TXIP / TXIN	UEM	HELGA	Differential voltage swing (static)	2.15	2.2	2.25	Vpp	Programmable voltage swing. Programmable common mode voltage. Between TXIP-TXIN
			DC level	1.17	1.20	1.23	V	
			Source Impedance			200	W	
TXQP / TXQN	UEM	HELGA	Same spec as for TXIP / TXIN					
AFC	UEM	VCTCXO	Voltage Min Max	0.0 2.4		0.1 2.6	V	Automatic frequency control signal for VCTCXO
			Resolution	11			bits	
			Load resistance and capacitance	1		 100	kΩ nF	
			Source Impedance			200	W	
TxC	UEM	HELGA	Voltage Min Max	 2.4		0.1	V	Transmitter power level and ramping control
			Source Impedance			200	W	
			Resolution	10			bits	
RFTemp	HELGA	UEM	Voltage at -20oC		1,57		V	Temperature sensor of RF.
			Voltage at +25oC		1,7			
			Voltage at +60oC		1,79			
DC_sense	PA	UEM	Voltage		0.6		V	PA final stage quiescent current level information
IPA1 / IPA2	UEM	PA	Output Voltage	0		2.7	V	PA final stage quiescent current adjustment
			Current range	0		5	mA	

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External Signals and Connections

Keyboard (board-to-board) Connector

Pin	Signal	Min.	Nom	Max	Condition	Note
1	GND		0V			
2	VLED+		VBAT 7.5V		LED off LED on	Supply Voltage for Key-board LEDs
3	ROW(4)	0.7xVIO 0		1.8V 0.3xVIO	High Low	Keyboard matrix row 4
4	ROW(3)	0.7xVIO 0		VIO 0.3xVIO	High Low	Keyboard matrix row 3
5	COL(2)	0.7xVIO 0		VIO 0.3xVIO	High Low	Keyboard matrix column 2
6	ROW(2)	0.7xVIO 0		VIO 0.3xVIO	High Low	Keyboard matrix row 2
7	COL(1)	0.7xVIO 0		VIO 0.3xVIO	High Low	Keyboard matrix column 1
8	ROW(0)	0.7xVIO 0		VIO 0.3xVIO	High Low	Keyboard matrix row 0
9	VLED1-		0V 1.9V		LED off LED on	LED Katode Voltage
10	ROW(1)	0.7xVIO 0		VIO 0.3xVIO	High Low	Keyboard matrix row 1
11	COL(3)	0.7xVIO 0		VIO 0.3xVIO	High Low	Keyboard matrix column 3
12	COL(4)	0.7xVIO 0		VIO 0.3xVIO	High Low	Keyboard matrix column 4
13	VLED2-		0V 1.9V		LED off LED on	LED Katode Voltage
14	GND		0V			
15	VLED3-		0V 1.9V		LED off LED on	LED Katode Voltage
16	GND		0V			

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LCD Connector (Board to Board)

Pin	Signal	Min.	Nom	Max	Condition	Note
1	VDDI	1.72V	1.8V	1.88V		Logic voltage supply Connected to VIO
2	XRES	0.7*VDDI 0		VDDI 0.3*VDDI	Logic '1' Logic '0'	Reset Active low
		1us			t_{rw}	Reset active
3	SI	0.7*VDDI 0		VDDI 0.3*VDDI	Logic '1' Logic '0'	Serial data
		100ns			t_{sds}	Data setup time
		100ns			t_{sdh}	Data hold time
4	SCLK	0.7*VDDI 0		VDDI 0.3*VDDI	Logic '1' Logic '0'	Serial clock input
				6.5MHz		Max frequency
		250ns			t_{scyc}	Clock cycle
		100ns			t_{shw}	Clock high
		100ns			t_{slw}	Clock low
5	CXS	0.7*VDDI 0		VDDI 0.3*VDDI	Logic '1' Logic '0'	Chip select Active low
		60ns			t_{css}	CXS low before SCLK rising edge
		100ns			t_{csh}	CXS low after SCLK rising edge
6	VLED+		VBAT 7.5V		LED off LED on	Supply Voltage for LEDs
7	VLED-		0V 0.525V		LED off LED on	Feedback Voltage to LED Driver
8	GND		0V	9V		Ground
9	NC					Not Connected

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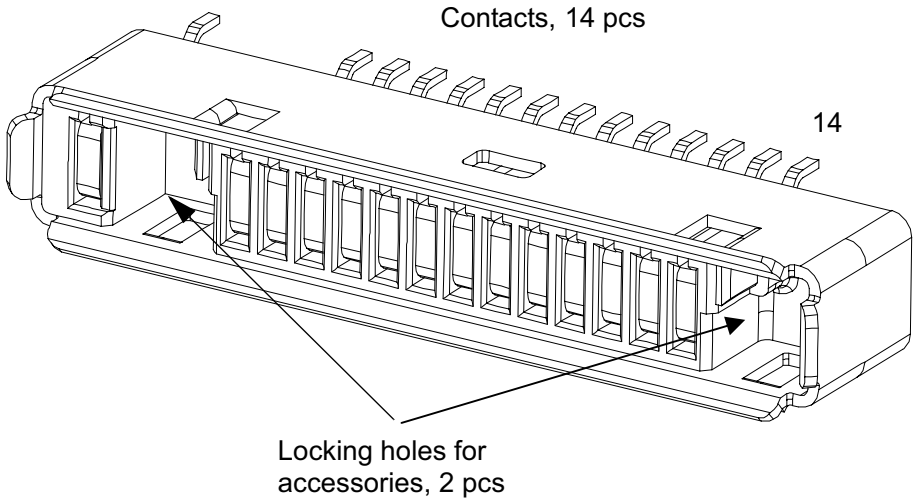
DC Connector

Pin	Signal	Min.	Nom	Max	Condition	Note
1	VCHAR		$11.1V_{peak}$	16.9 V_{peak} 7.9 V_{RMS} 1.0 A_{peak}	Standard charger	Charger positive input
		7.0 V_{RMS}	8.4 V_{RMS}	9.2 V_{RMS} 850 mA	Fast charger	
2	CHGND		0			Charger ground

Bottom Connector

Bottom connector, or the system connector is of type Pop-Port (TM)

Figure 4: Bottom connector pinout



Bottom connector pins and signals:

Pin/ Signal name	Signal description	Spectral range	Voltage / Current levels	Max or nominal serial impedance	Note
1	CHARGE	V Charge	DC	0-9 V / 0.85 A	
2	GND	Charge GND		0.85 A	(PWB + conn.)
3	ACI	ACI	1 kbit/s	Dig 0 / 2.78V	Insertion & removal detection
4	VOUT	DC out	DC	2.78V / 70mA	(PWB + conn.) 200mW
5	NC				Not connected
6	FBUS RX		FBUS 115kbit	0 / 2.78V	
7	FBUS TX		FBUS 115kbit	0 / 2.78V	

8	GND	Data GND			
9	XMIC N	Audio in	300 - 8k	1Vpp & 2.78V	Ext. Mic Input
10	XMIC P	Audio in	300 - 8k	1Vpp & 2.78V	Ext. Mic Input
11	HSEAR N	Audio out	20 - 20k	1Vpp	Ext. audio out (left)
12	HSEAR P	Audio out	20 - 20k	1Vpp	Ext. audio out (left)
13	HSEAR R N	Audio out	20 - 20k	1Vpp	Ext. audio out (right)
14	HSEAR R P	Audio out	20 - 20k	1Vpp	Ext. audio out (right)

SIM connector

Pin	Name	Parameter	Min.	Typ	Max	Unit	Notes
1	VSIM	1.8V SIM Card	1.6	1.8	1.9	V	Supply voltage
		3V SIM Card	2.8	3.0	3.2	V	
2	SIMRST	1.8V SIM Card	0.9xVSIM 0		VSIM 0.15xVSIM	V	SIM reset (output)
		3V SIM Card	0.9xVSIM 0		VSIM 0.15xVSIM	V	
3	SIMCLK	Frequency		3.25		MHz	SIM clock
		Trise/Tfall			50	ns	
		1.8V Voh 1.8V Vol	0.9xVSIM 0		VSIM	V	
		3V Voh 3V Vol	0.9xVSIM 0		VSIM	V	
4	DATA	1.8V Voh 1.8V Vol	0.9xVSIM 0		VSIM 0.15xVSIM	V	SIM data (output)
		3V Voh 3V Vol	0.9xVSIM 0		VSIM 0.15xVSIM		
		1.8V Vih 1.8V Vil	0.7xVSIM 0		VSIM 0.15xVSIM	V	SIM data (input) Trise/Tfall max 1us
		3V Vil 3V Vil	0.7xVSIM 0		VSIM 0.15xVSIM		
5	NC						Not connected
6	GND	GND	0		0	V	Ground

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Internal Signals and Connections

Internal microphone

Signal		Min.	Nom	Max	Condition	Note
MICP			200mV$_{pp}$	AC	2.2kΩ to MIC1B	MICP
	2.0 V	2.1 V	2.25 V	DC		
MICN	2.0V	2.1V	2.25V	DC		MICN

Internal speaker

Signal		Min.	Nom	Max	Condition	Note
EARP	0.75V	0.8V	2.0 V$_{pp}$ 0.85V	AC DC	Differential output (V$_{diff}$ = 4.0 V$_{pp}$)	EARP
EARN	0.75V	0.8V	2.0 V$_{pp}$ 0.85V	AC DC		EARN

Integrated HF speaker

Signal		Min.	Nom	Max	Condition	Note
IHFP	0.75V	0.8V	2.0 V$_{pp}$ 0.85V	AC DC	Differential output (V$_{diff}$ = 4.0 V$_{pp}$)	IHFP
IHFN	0.75V	0.8V	2.0 V$_{pp}$ 0.85V	AC DC		IHFN

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Baseband Functional Description

Modes of Operation

TB3 baseband has six different functional modes:

- No supply
- Back-up
- Acting Dead
- Active
- Sleep
- Charging

No Supply

In NO_SUPPLY mode, the phone has no supply voltage. This mode is due to disconnection of main battery and backup battery or low battery voltage level in both of the batteries.

Phone is exiting from *NO_SUPPLY* mode when sufficient battery voltage level is detected. Battery voltage can rise either by connecting a new battery with $VBAT > V_{MSTR+}$ or by connecting charger and charging the battery above V_{MSTR+}.

Back-up

In *BACK_UP* mode the backup battery has sufficient charge but the main battery can be disconnected or empty ($VBAT < V_{MSTR}$ *and* $VBACK > VBU_{COFF}$).

VRTC regulator is disabled in *BACK_UP* mode. VRTC output is supplied without regulation from backup battery (VBACK). All the other regulators are disabled in *BACK_UP* mode.

Acting Dead

If the phone is off when the charger is connected, the phone is powered on but enters a state called "*Acting Dead*". To the user, the phone acts as if it was switched off. A battery charging alert is given and/or a battery charging indication on the display is shown to acknowledge the user that the battery is being charged.

Active

In the *Active* mode the phone is in normal operation, scanning for channels, listening to a base station, transmitting and processing information. There are several sub-states in the active mode depending on if the phone is in burst reception or burst transmission.

One of the sub-states of the active mode is FM radio on state. In that case, Audio Amplifier and FM radio are powered on. FM radio circuitry is controlled by the MCU and 13MHz-reference clock is generated in the UPP. VFLASH2 regulator is operating.

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In *Active* mode the RF regulators are controlled by SW writing into EM's registers wanted settings: VR1A can be enabled or disabled. VR2 can be enabled or disabled and its output voltage can be programmed to be 2.78V or 3.3V. VR4 -VR7 can be enabled, disabled, or forced into low quiescent current mode. VR3 is always enabled in Active mode.

Sleep Mode

Sleep mode is entered when both MCU and DSP are in stand–by mode. Sleep is controlled by both processors. When SLEEPX low signal is detected UEM enters SLEEP mode. VCORE, VIO and VFLASH1 regulators are put into low quiescent current mode. All the RF regulators are disabled in SLEEP. When SLEEPX=1 detected UEM enters ACTIVE mode and all functions are activated.

The sleep mode is exited either by the expiration of a sleep clock counter in the UEM or by some external interrupt, generated by a charger connection, key press, headset connection etc.

In sleep mode VCTCXOr is shut down and 32 kHz sleep clock oscillator is used as reference clock for the baseband.

Charging

Charging can be performed in any operating mode.

NHL-4J/NHL-4JX supports the standard NMP charger interface.

Supported chargers are ACP-7, ACP-8, ACP-9, ACP-12, LCH-8 and LCH-9.

Charging is controlled by the UEM ASIC and external components are needed for EMC, reverse polarity and transient protection of the input to the baseband module. The charger connection is through the system connector interface. The NHL-4J/NHL-4JX baseband is designed to support DCT3 chargers from an electrical point of view. Both 2- and 3-wire type chargers are supported.

The operation of the charging circuit has been specified in such a way as to limit the power dissipation across the charge switch and to ensure safe operation in all modes.

Battery

720 mAh Li-ion battery pack BLD-3 is used in NHL-4J/NHL-4JX.

Description	Value
Nominal discharge cut-off voltage	3.1V
Nominal battery voltage	3.6V
Nominal charging voltage	4.2V
Maximum charger output current	850 mA
Minimum charger output current	200 mA

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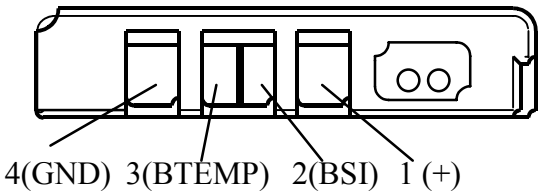
Pin numbering of battery pack

Signal name	Pin number	Function
VBAT	1	Positive battery terminal
BSI	2	Battery capacity measurement (fixed resistor inside the battery pack)
BTEMP	3	Battery temperature measurement (measured by ntc resistor inside pack)
GND	4	Negative/common battery terminal

BLD-3 battery pack pin order

Figure 5:



Power Up and Reset

Power up and reset is controlled by the UEM ASIC. NHL-4J/NHL-4JX baseband can be powered up in following ways:

- Press power button which means grounding the PWRONX pin on UEM
- Connect the charger to the charger input
- Supply battery voltage to the battery pin.
- RTC Alarm, the RTC has been programmed to give an alarm

After receiving one of the above signals, the UEM counts a 20ms delay and then enters its reset mode. The watchdog starts up, and if the battery voltage is greater than Vcoff+, a 200ms delay is started to allow references etc. to settle. After this delay elapses the VFLASH1 regulator is enabled.

500us later VR3, VANA, VIO and VCORE are enabled. Finally the PURX line is held low for 20 ms. This reset, PURX, is fed to the baseband ASIC UPP, resets are generated for the DSP and the MCU. During this reset phase the UEM forces the VCXO regulator on regardless of the status of the sleep control input signal to the UEM.

The sleep signal from the ASIC is used to reset the flash during power up and to put the flash in power down during sleep. All baseband regulators are switched on at the UEM power on except for the SIM regulator that is controlled by the MCU. The UEM internal

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watchdog is running during the UEM reset state, with the longest watchdog time selected. If the watchdog expires, the UEM returns to power off state. The UEM watchdog is internally acknowledged at the rising edge of the PURX signal in order to always give the same watchdog response time to the MCU.

Power Up with PWR key

When the Power on key is pressed the UEM enters the power up sequence as described in the previous paragraph. Pressing the power key causes the PWRONX pin on the UEM to be grounded. The UEM PWRONX signal is not part of the keypad matrix. The power key is only connected to the UEM. This means that when pressing the power key an interrupt is generated to the UPP that starts the MCU.

The MCU then reads the UEM interrupt register and notices that it is a PWRONX interrupt. The MCU now reads the status of the PWRONX signal using the UEM control bus, CBUS. If the PWRONX signal stays low for a certain time the MCU accepts this as a valid power on state and continues with the SW initialization of the baseband. If the power on key does not indicate a valid power on situation, the MCU powers off the baseband.

Power Up when Charger is connected

In order to be able to detect and start charging in a case where the main battery is fully discharged (empty) and hence UEM has no supply (NO_SUPPLY or BACKUP mode of UEM), charging is controlled by START-UP CHARGING circuitry.

Whenever VBAT level is detected to be below master reset threshold (VMSTR-) charging is controlled by START_UP charge circuitry. Connecting a charger forces VCHAR input to rise above charger detection threshold, VCHDET+.

By detection start-up charging is started. UEM generates 100mA constant output current from the connected charger's output voltage. As battery charges its voltage rises, and when VBAT voltage level higher than master reset threshold limit (VMSTR+) is detected START_UP charge is terminated.

Monitoring the VBAT voltage level is done by charge control block (CHACON). MSTRX='1' output reset signal (internal to UEM) is given to UEM's RESET block when VBAT>VMSTR+ and UEM enters into reset sequence described in section Power Up and Reset.

If VBAT is detected to fall below VMSTR- during start-up charging, charging is cancelled. It will restart if new rising edge on VCHAR input is detected (VCHAR rising above VCHDET+).

Power Up when Battery is connected

Baseband can be powered up by connecting battery with sufficient voltage. Battery voltage has to be over UEM internal comparator threshold level, Vcoff+. Battery low limit is specified in Table 2. Battery Voltage Range. When battery voltage is detected, UEM enters to reset sequence as described in section Power Up and Reset

Phone can be powered up to LOCAL mode by setting BSI resistor 560Ω. This causes MCU to wake up directly when battery voltage is supplied.

RTC Alarm Power Up

If phone is in power off mode when RTC alarm occurs the wake up procedure is as described in section Power Up and Reset. After baseband is powered on, an interrupt is given to MCU. When RTC alarm occurs during power on state the interrupt for MCU is generated.

A/D Channels

The UEM contains the following A/D converter channels that are used for several measurement purpose. The general slow A/D converter is a 10 bit converter using the UEM interface clock for the conversion. An interrupt will be given at the end of the measurement.

The UEM's 11-channel analog to digital converter is used to monitor charging functions, battery functions, user interface and RF functions.

The monitored battery functions are battery voltage (VBATADC), battery type (BSI) and battery temperature (BTEMP) indication.

The battery type is recognized through a resistive voltage divider. In phone there is a 100kΩ pull up resistor in the BSI line and the battery has a pull down resistor in the same line. Depending on the battery type the pull down resistor value varies. The battery temperature is measured in the same way except that the battery has a NTC pull down resistor in the BTEMP line.

KEYB1&t2 inputs are used for keyboard scanning purposes. These inputs are also routed internally to the miscellaneous block.

The monitored RF functions are PATEMP and VCXOTEMP detection. PATEMP input is used to measure temperature of the RFIC, the Helga.

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FM Radio

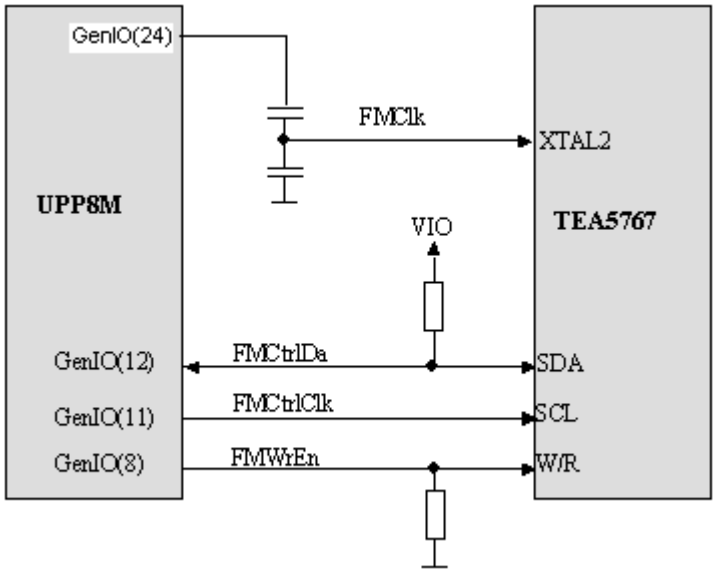
The FM radio in the transceiver NHL-4J/NHL-4JX is a single chip electronically tuned FM srereo radio with fully integrated IF selectivity and demodulation. The FM radio is completely adjustment free.

It can be tuned into the European FM bands.

The channel tuning and bus data are controlled by UPP. A variable capacitance diode, two coils and some resistors and capacitors are the external components for the FM radio.

The audio frequency is fed via UEM to a headset of the phone. The FM radio antenna is implemented in a cable of the headset.

Figure 6: FM radio



IR Module

The IR interface is designed into the UPP. The IR link supports speeds from 9600 bit/s to 1.152 MBit/s up to distance of 80 cm. Transmission over the IR if half-duplex.

SIM Interface

UEM contains the SIM interface logic level shifting. SIM interface can be programmed to support 3V and 1.8V SIMs. SIM supply voltage is selected by a register in the UEM. It is only allowed to change the SIM supply voltage when the SIM IF is powered down.

The SIM power up/down sequence is generated in the UEM. This means that the UEM generates the RST signal to the SIM. Also the SIMCardDet signal is connected to UEM. The card detection is taken from the BSI signal, which detects the removal of the battery.

The SIM interface is powered up when the SIMCardDet signal indicates "card in". This

signal is derived from the BSI signal.

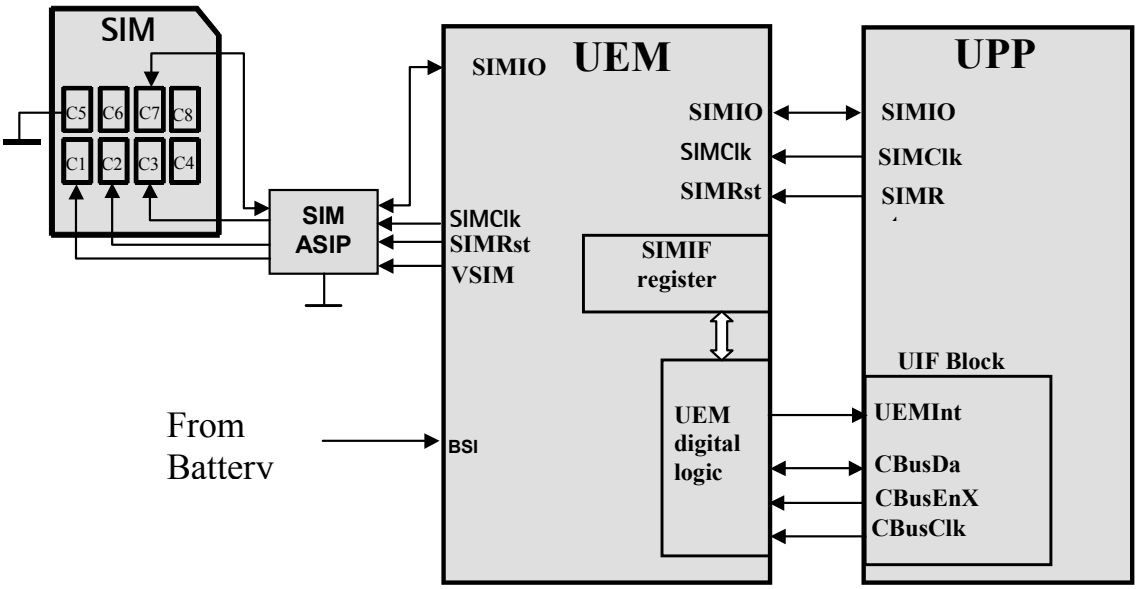
Parameter	Variable	Min.	Typ	Max	Unit
SIMCARDet, BSI comparator Threshold	Vkey	1.94	2.1	2.26	V
SIMCARDet, BSI comparator Hysteresis (1)	Vsimhyst	50	75	100	mV

The entire SIM interface locates in two chips: UPP and UEM.

The SIM interface in the UEM contains power up/down, port gating, card detect, data receiving, ATR-counter, registers and level shifting buffers logic. The SIM interface is the electrical interface between the Subscriber Identity Module Card (SIM Card) and mobile phone (via UEM device).

The data communication between the card and the phone is asynchronous half duplex. The clock supplied to the card is 1.083 MHz or 3.25 MHz.

Figure 7: SIM interface NHL-4J/NHL-4JX



ACI

ACI is a point-to-point, bi-directional serial bus. ACI has two main features: **1**)The insertion and removal detection of an accessory device **2**) acting as a data bus, intended mainly for control purposes. A third function provided by ACI is to identify and authenticate the specific accessory which is connected to the System interface.

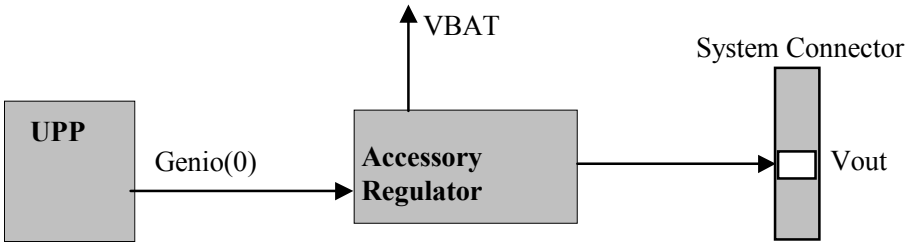
External Accessory Regulator

An external LDO Regulator exists for accessory power supply purposes. All ACI-accessories require this power supply. Regulator input is connected to battery voltage VBAT and output is connected to Vout pin in the system connector. Regulator is controlled via UPP (On/Off-function).

Accessory Regulator Signals

Signal	Min.	Nom	Max	Note
Vout	2.70V	2.78	2.86V	I_{max} = 150mA
GenIO(0)	1.4	1.8	1.88 0.6	High (ON) Low (OFF)

Figure 8: External Accessory regulation



External Audio

NHL-4J/NHL-4JX is designed to support fully differential external audio accessory connection by using Pop-Port [TM] system connector. Pop-Port [TM] connector has serial data bus called ACI (Accessory Control Interface) for accessory insertion and removal detection and identification and authentication. ACI line is also used for accessory control purposes. See section ACI, Accessory Control Interface. Audio support from Pop-Port [TM] system connector:

4-wire fully differential stereo audio (used also FM-radio antenna connection)

2-wire differential mic input

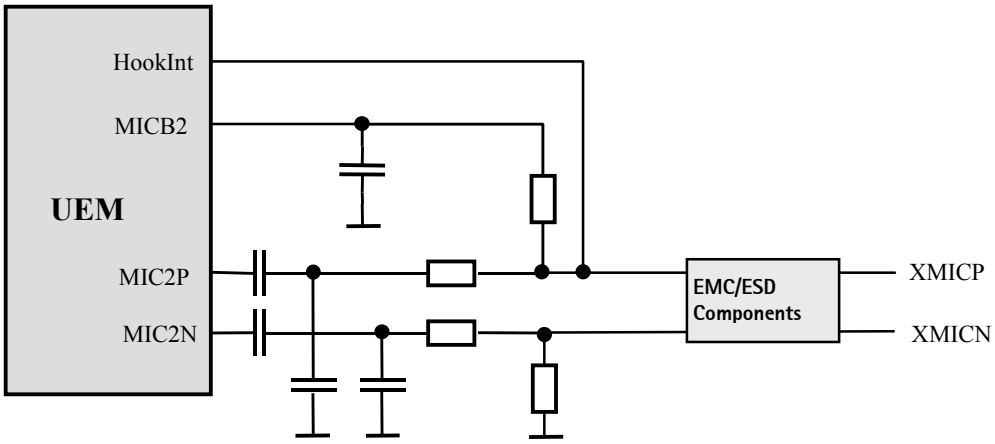
External Microphone Connection

The external microphone input is fully differential and lines are connected to the UEM microphone input MIC2P/N. The UEM (MICB2) provides bias voltage. Microphone input lines are ESD protected.

Creating a short circuit between the headset microphone signals generates the hook signal. When the accessory is not connected, the UEM resistor pulls up the HookInt signal. When the accessory is inserted and the microphone path is biased the HookInt signal decreases to 1.8V due to the microphone bias current flowing through the resistor. When the button is pressed the microphone signals are connected together, and the HookInt input will get half of micbias dc value 1.1 V. This change in DC level will cause the Hook-

Int comparator output to change state, in this case from 0 to 1. The button can be used for answering incoming calls but not to initiate outgoing calls.

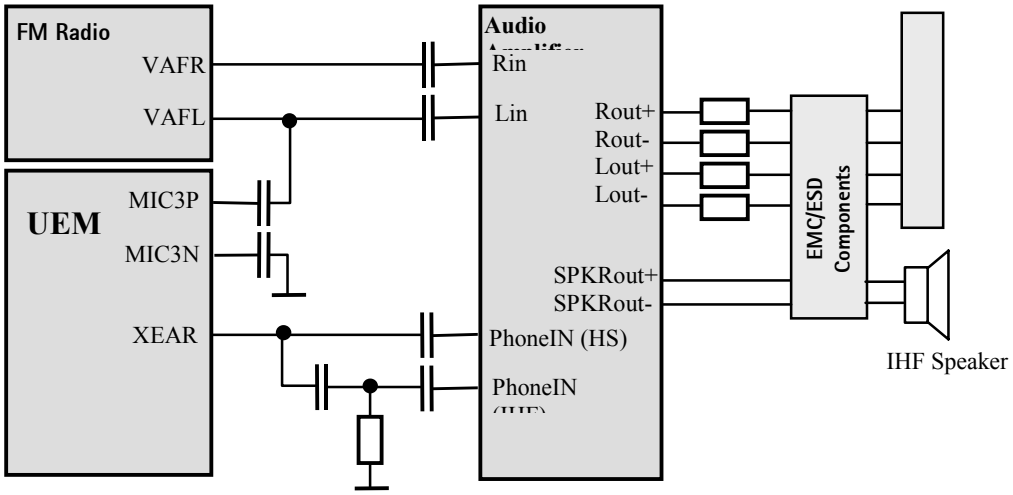
Figure 9: External microphone connection



External Earphone Connections

Headset implementation uses separate microphone and earpiece signals. The accessory is detected by the HeadInt signal when the plug is inserted (see section ACI, Accessory Control Interface).

Figure 10: Figure 22 External Earphone & IHF Connections



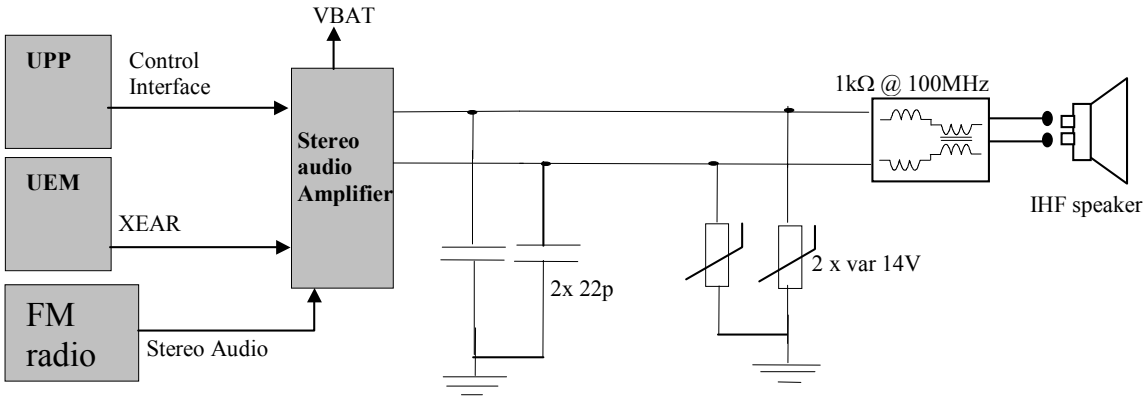
When the accessory is inserted and the microphone path is biased the HookInt signal decreases to 1.8V due to the microphone bias current flowing through the resistor. When the button is pressed the microphone signals are connected together, and the HookInt input will get half of micbias dc value 1.1 V. This change in DC level will cause the Hook-Int comparator output to change state, in this case from 0 to 1. The button can be used for answering incoming calls but not to initiate outgoing calls.

Internal Audio

IHF Speaker & Stereo Audio Amplifier

Integrated Hands Free Speaker, 16mm MALT, is used to generate speech audio, alerting and warning tones in NHL-4J/NHL-4JX. Audio amplifier is controlled by the UPP. Speaker capsule is mounted in the C-cover. Spring contacts are used to connect the IHF Speaker contacts to the main PWB.

Figure 11: IHF speaker and amplifier



Internal Microphone

The internal microphone capsule is mounted to in the UI-frame. The microphone is omni-directional and it's connected to the UEM microphone input MIC1P/N. The microphone input is asymmetric and the UEM (MICB1) provides bias voltage. The microphone input on the UEM is ESD protected. Spring contacts are used to connect the microphone to the mainPWB.

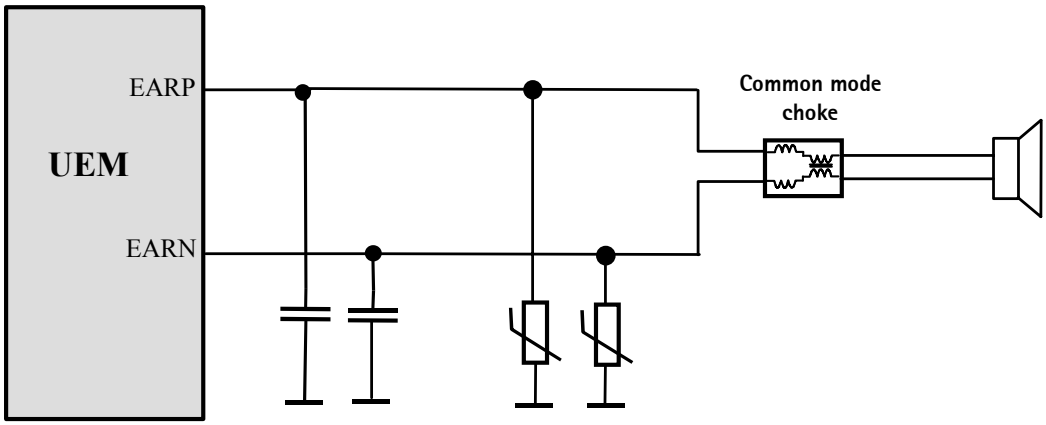
Figure 12: Internal microphone

Internal Speaker

The internal earpiece is a dynamic earpiece with impedance of 32 ohms. The earpiece must be low impedance one since the sound pressure is to be generated using current and not voltage as the supply voltage is restricted to 2.7V. The earpiece is driven directly

by the UEM and the earpiece driver in UEM is a bridge amplifier. In NHL-4J/NHL-4JX 8mm PICO type earpiece is used.

Figure 13: Internal speaker



IHF Speaker & Stereo Audio Amplifier

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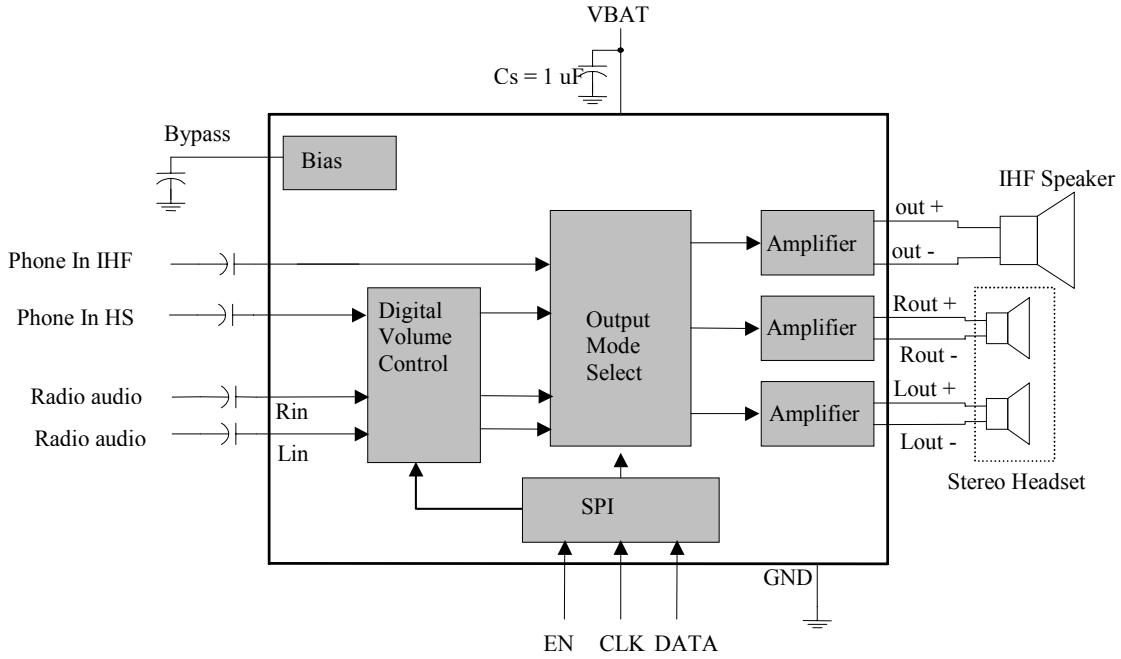
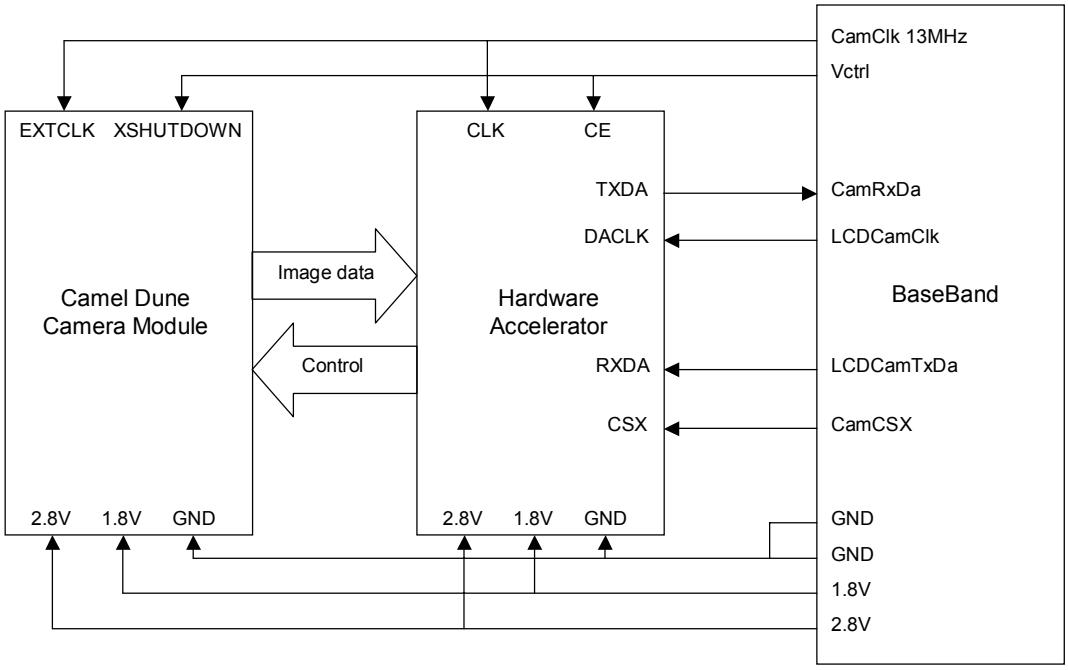
Figure 14: Digital Interface of Audio Amplifier



Camera

Camera is connected to the BB by UIF –bus. UIF is a slow (10MHz bus) which may be shared with other UI functions (e.g. LCD). This version has unidirectional TX and Rx data lines and consists of a chip enable, chip select, Tx data, Rx data, data clock and system clock. Note there is a severe restriction on image transfer in UPP v2 devices due to a DMA shortcoming. A block transfer mode is available to workaround this but the performance in frame rate terms will not be brilliant.

Figure 15: Camera and HWA connections to the baseband using UIF bus



Signal descriptions

Chip-select **CSX** enables and disables the camera serial bus. **CSX** is active low. An additional function of **CSX** during the power up sequence is to determine the communication mode of the HWA (UIF or CCI/CCP).

DaClk is a serial data clock and is typically set to ExtClk/2. The clock can be driven low when data is not transmitted, but may be running when **CSX** is inactive as well.

RxDa data-length is 8 bits + **D/C-bit**. The first bit to be received is **D/C-bit** which indicates to the camera the status of following 8 bit data. In the case of command data to camera the **D/C-bit** is low ('0'). The camera must not react to received data if **D/C-bit** is high ('1').

TxDa data-length is 8 bits + **TxEnd-bit**. The first bit to be transmitted is the **TxEnd-bit** which indicates if the data is the last byte from image frame. When a byte is the last byte of an image frame from the camera, the **TxEnd**-bit is set high ('1'). Otherwise the **TxEnd**-bit is set low ('0') by the camera. The camera can interrupt the baseband by driving **TxDa** low for at least one **ExtClk** cycle when not transferring an image. The interrupt is initiated by the falling edge of the signal.

ExtClk is external system clock for the camera module. The clock may be AC or DC coupled. Four fixed frequencies are available (8.4, 9.6, 9.72,13 and 16.8 MHz each within +/-100kHz).

VCAMDIG is a regulated 1.8V nominal I/O logic supply for the HWA and sensor. Regulator output voltages are seen in **Table 5**. Global net is named VCAMDIG in schematics and connected to the sensor's and HWA's VIO –interface.

VCtrl is a control signal to place the camera and HWA in their lowest power consumption modes. It must be permissible to pull this signal up if this functionality is not required.

VANA is a regulated 2.78V nominal voltage from the engine to the camera module.

GND is system GND for camera module.

Memory Block

For the MCU UPP includes ROM, 2 Kbytes, that is used mainly for boot code of MCU. To speed up the MCU operation small 64-byte cache is also integrated as a part of the MCU memory interface.

For program memory 8Mbit (512 x 16bit) PDRAM is integrated. RAM block can also be used as data memory and it is byte addressable. RAM is mainly for MCU purposes but also DSP has also access to it if needed.

MCU code is stored into external flash memory. Size of the flash is 128Mbit (8k x 16bit) The HDb16 baseband supports a burst mode flash with multiplexed address/data bus. Access to the flash memory is performed as 16-bit access. The flash has Read While Write capabilities, which makes the emulation of EEPROM within the flash easy.

Security

The phone flash program and IMEI codes are software protected using an external security device that is connected between the phone and a PC.

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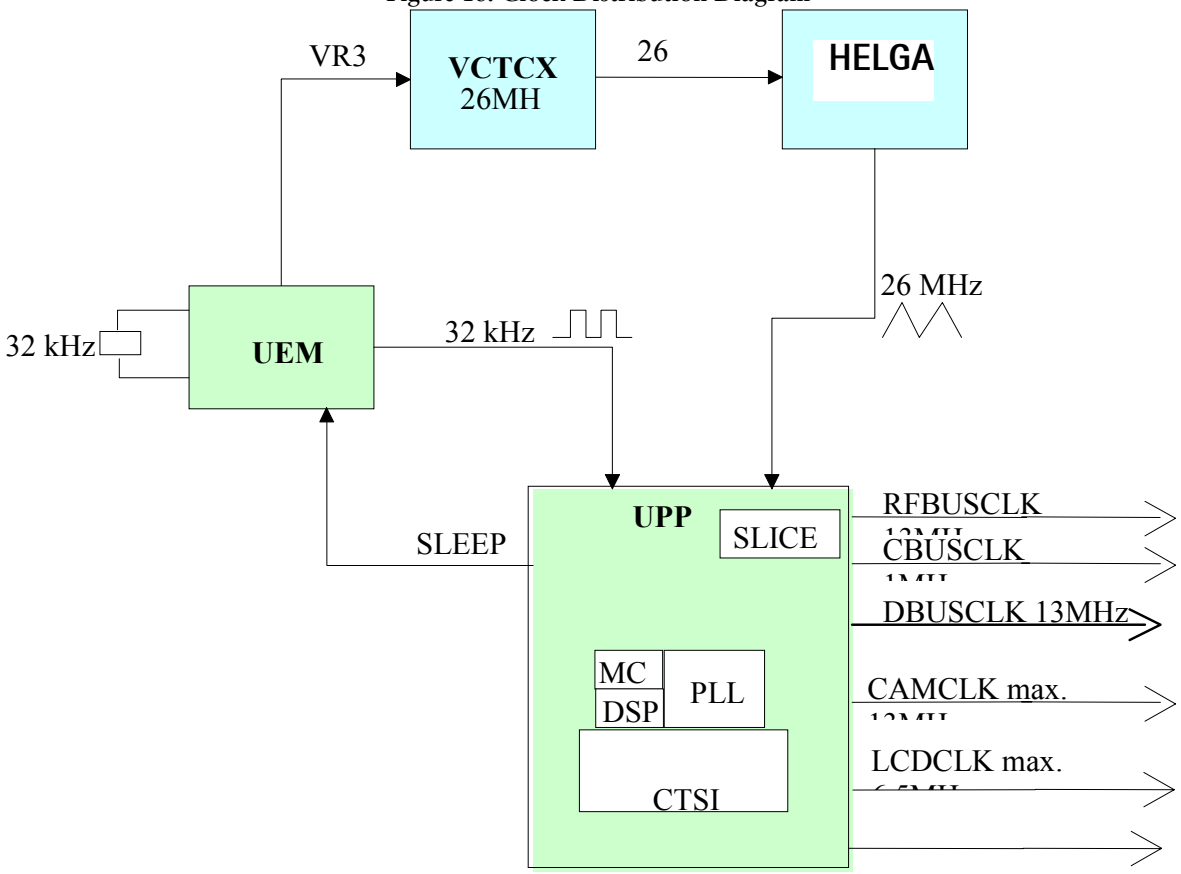
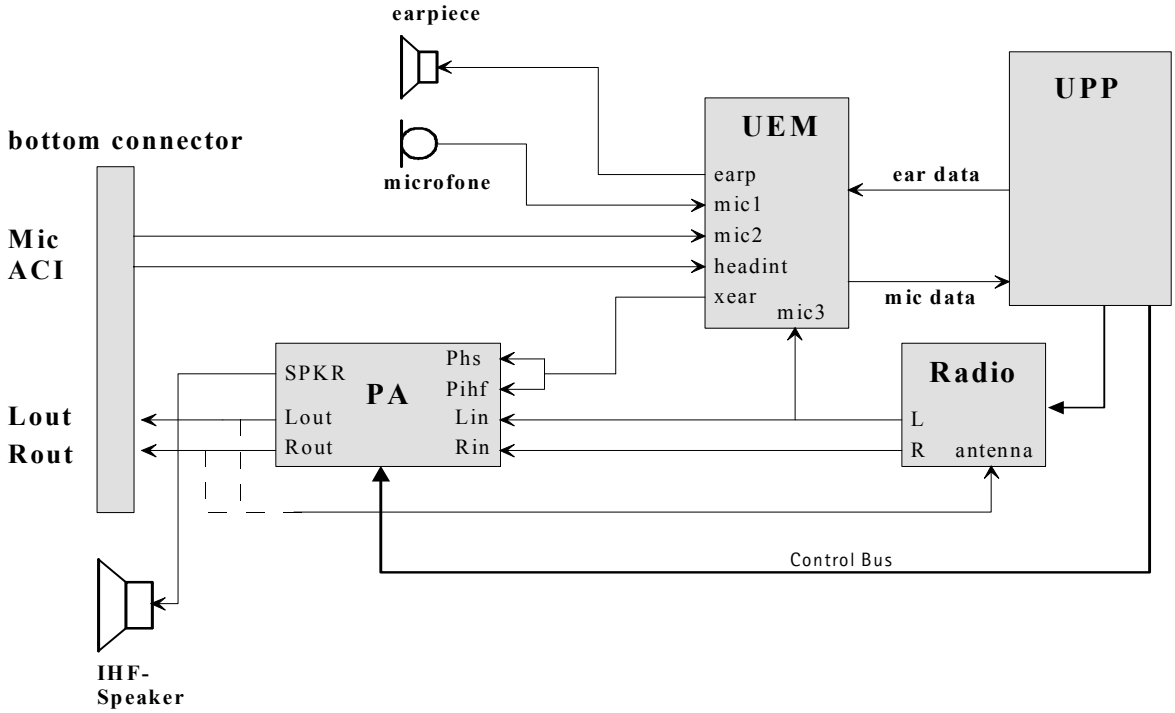
Clock Distribution

Figure 16: Clock Distribution Diagram



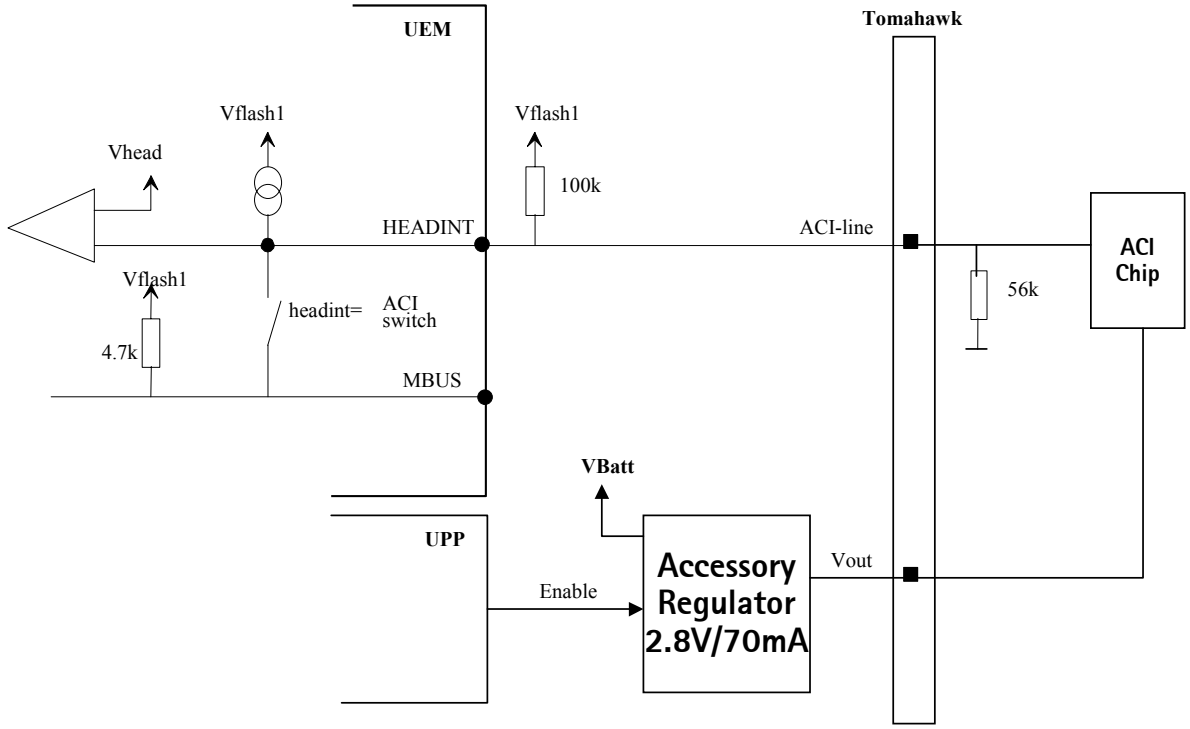
Audio Control

Figure 17: Audio block diagram NHL-4J/NHL-4JX



Accessory identification and Power Supply

Figure 18: Accessory identification and Power supply



Backup Battery

Backup battery is used in case when main battery is either removed or discharged. Backup battery is used for keeping real-time clock running for minimum of 30 minutes.

Rechargeable backup battery is connected between UEM VBACK and GND. In UEM backup battery charging high limit is set to 3.2V. The cut–off limit voltage (V BUCoff–) for backup battery is 2.0V. Backup battery charging is controlled by MCU by writing into UEM register.

Li-Ion SMD battery type is used. The nominal capacity of the battery is 0.01 mAh.

Table 28. Backup Battery circuitry

Parameter Test conditions	Symbol	Min	Typ	Max	Units
Back-up battery voltage	VBACK	2.43		3.3	V
Back-up battery cut-off limit	V_BU_{COFF+} V_BU_{COFF-}	2.04 1.94	2.10 2.0	2.16 2.06	V V
Charging voltage (VBAT ? 3.4V)	VBU	3.1	3.2	3.3	V
Charging current	I_{LIMVBU}	150		500	mA

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RF Module Introduction

The RF module performs the necessary high frequency operations of the EGSM900/ DCS1800/PCS1900 tripleband engine. Both the transmitter and receiver have been implemented by using direct conversion architecture which means that the modulator and demodulator operate at the channel frequency.

The core of the RF is an application-specific integrated circuit, Helga. Another core component is a power amplifier module which includes two amplifier chains, one for EGSM900 and the other for DCS1800/PCS1900.

Other key components include

- 26 MHz VCTCXO for frequency reference
- 3420-3980 MHz SHF VCO (super high frequency voltage controlled oscillator)
- front end module comprising a RX/TX switch and two RF bandpass SAW filters
- three additional SAW filters

The control information for the RF is coming from the baseband section of the engine through a serial bus, referred later on as RFBus. This serial bus is used to pass the information about the frequency band, mode of operation, and synthesizer channel for the RF. In addition, exact timing information and receiver gain settings are transferred through the RFBus. Physically, the bus is located between the baseband ASIC called UPP and Helga. Using the information obtained from UPP Helga controls itself to the required mode of operation and further sends control signals to the front end and power amplifier modules. In addition to the RFBus there are still other interface signals for the power control loop and VCTCXO control and for the modulated waveforms.

RF circuitry is located on one side of the 8 layer PWB.

EMC leakage is prevented by using a metal cans. The RF circuits are separated to three blocks.

- FM radio.
- PA, front end module, LNA and 1900 band SAWs.
- Helga RF IC, VCO, VCTCXO, baluns and balanced filters.

The RF transmission lines constitute of striplines and microstriplines after PA.

The baseband circuitry is located on the one side of the board, which is shielded with a metallized frame and ground plane of the UI-board.

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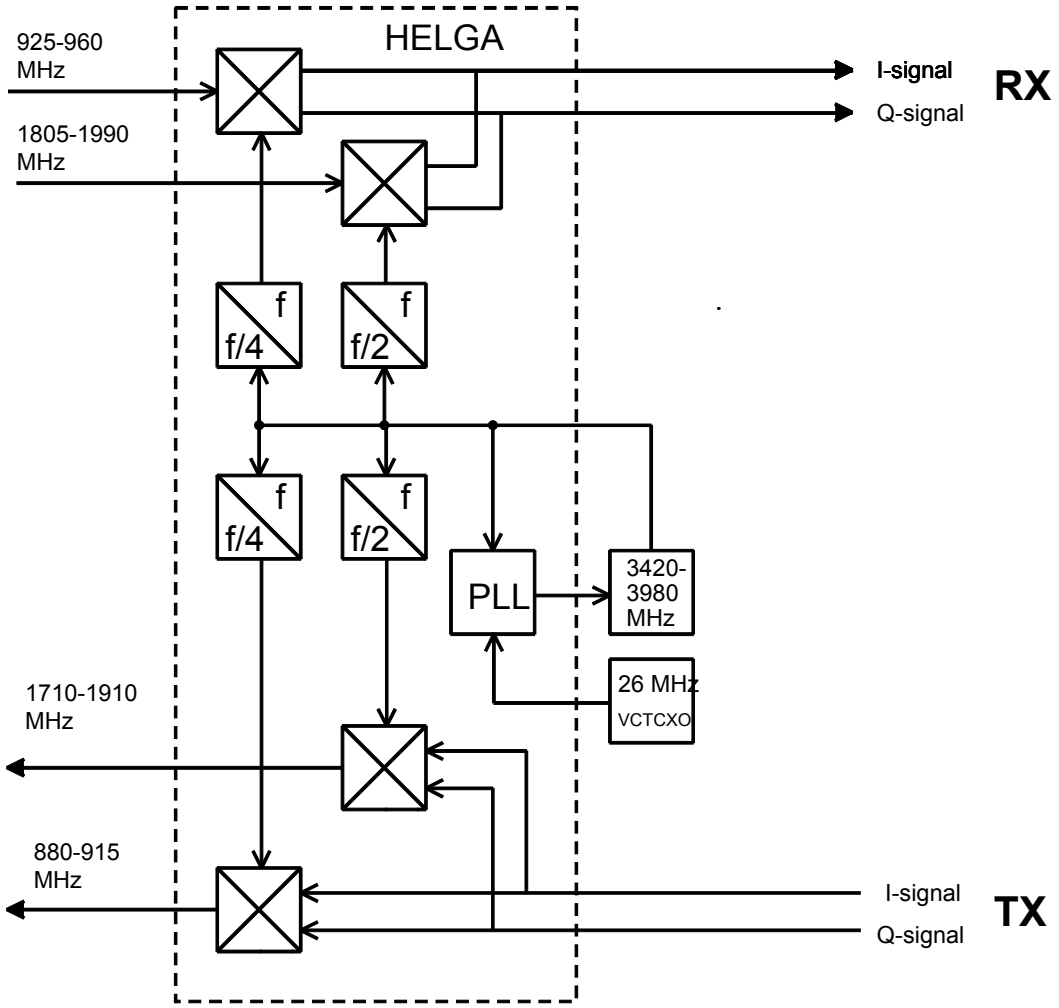
RF Frequency Plan

RF frequency plan is shown below. The VCO operates at the channel frequency multiplied by two or four depending on the frequency band of operation. This means that the base-band modulated signals are directly converted up to the transmission frequency and the received RF signals directly down to the baseband frequency.

Figure 19: RF Frequency plan



DC characteristics

Regulators

The transceiver baseband section has a multi function analog ASIC, UEM, which contains among other functions six pieces of 2.78 V linear regulators and a 4.8 V switching regulator. All the regulators can be controlled individually by the 2.78 V logic directly or through a control register. Normally, direct control is needed because of switching speed requirement: the regulators are used to enable the RF-functions which means that the controls must be fast enough.

The use of the regulators can be seen in the power distribution diagram which is presented in Figure 20, "Power distribution diagram," on page 48.

The seven regulators are named VR1 to VR7. VrefRF01 and VrefRF02 are used as the reference voltages for the Helga, VrefRF01 (1.35V) for the bias reference and VrefRF02 (1.35V) for the RX ADC (analog-to-digital converter) reference.

The regulators (except for VR7) are connected to the Helga. Different modes of operation can be selected inside the Helga according to the control information coming through the RFBus.

List of the needed supply voltages

Volt. source	Load
VR1	PLL charge pump (4.8 V)
VR2	TX modulators, ALCs, driver
VR3	VCTCXO, synthesizer digital parts
VR4	Helga pre-amps, mixers, DtoS
VR5	dividers, LO-buffers, prescaler
VR6	LNAs, Helga baseband (Vdd_bb)
VR7	VCO
VrefRF01	ref. voltage for Helga
VrefRF02	ref. voltage for Helga
Vbatt	PA

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Typical current consumption

The table shows the typical current consumption in different operation modes.

Operation mode	Current consumption	Notes
Power OFF	< 10 uA	Leakage current (triple band PA)
RX, EGSM900	75 mA, peak	
RX, DCS1800/PCS1900	70 mA, peak	
TX, power level 5, EGSM900	1700 mA, peak	
TX, power level 0, DCS1800/PCS1900	1000 mA, peak	

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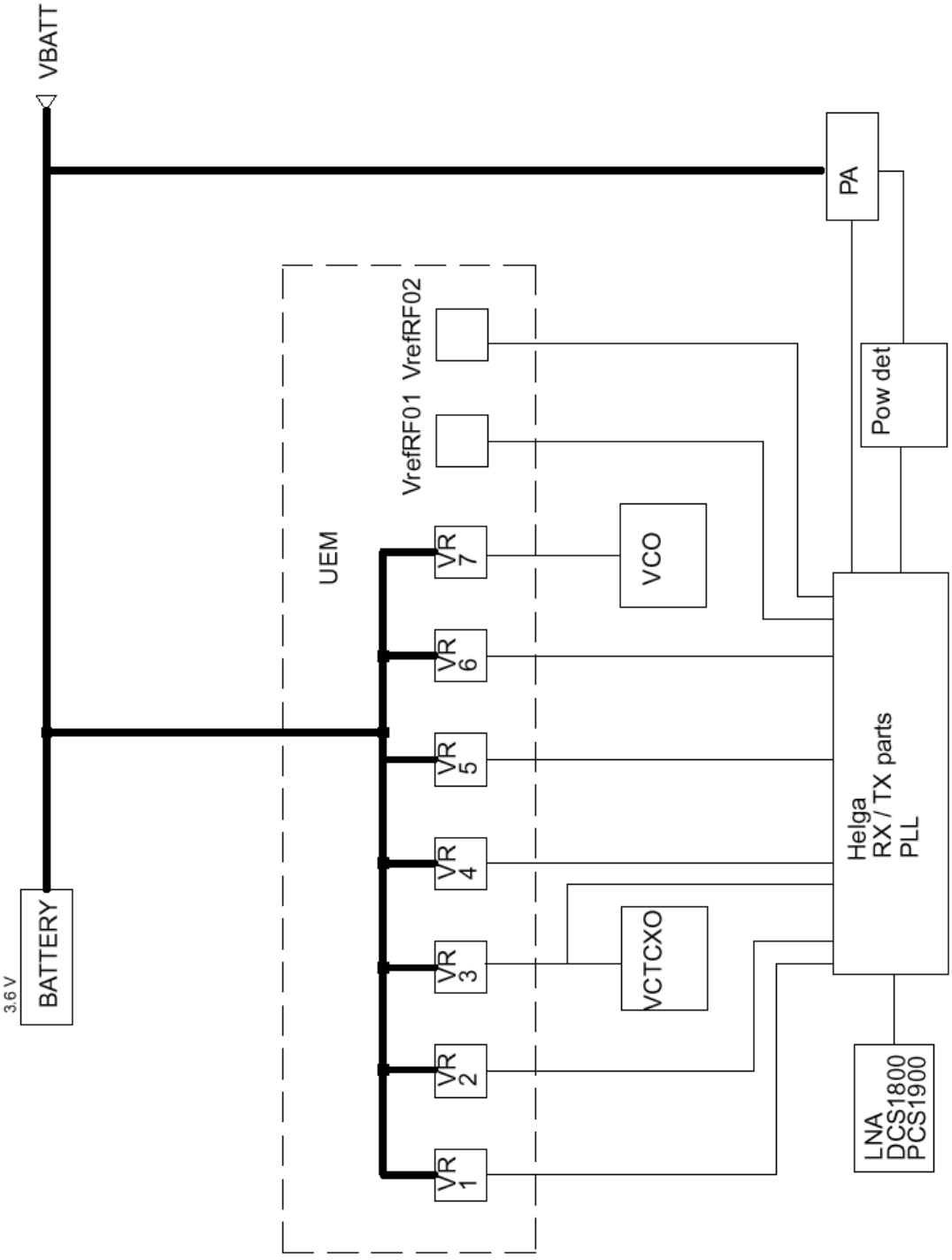
Power Distribution

Figure 20: Power distribution diagram



RF characteristics

Channel Numbers and Frequencies

System	Channel number	TX frequency	RX frequency	Unit
EGSM	0 <= n <=124	F = 890 + 0.2 * n	F = 935 + 0.2 * n	MHz
	975 <= n <= 1023	F= 890+0.2* (n -1024)	F= 935+0.2* (n -1024)	MHz
DCS1800	512 <= n <= 885	F=1710.2+0.2*(n-512)	F=1805.2+0.2*(n-512)	MHz
PCS1900	512 <= n <=810	F=1850.2+0.2*(n-512)	F=1930.2+0.2*(n-512)	MHz

Main RF characteristics

Parameter	Unit and value
Cellular System	GSM900, DCS1900 and PCS1900
RX Frequency Band	EGSM: 925 - 935 MHz GSM900: 935 - 960 MHz DCS1900: 1805 - 1880 MHz PCS1900: 1930 - 1990 MHz
TX Frequency Band	EGSM: 880 - 890 MHz GSM900: 890 - 915 MHz DCS1900: 1710 - 1785 MHz PCS1900: 1850 - 1910 MHz
Output Power	EGSM900: +5...+33 dBm / 3.2 mW... 2 W DCS1900: +0...+30 dBm / 1.0 mW... 1 W PCS1900: +0...+30 dBm / 1.0 mW... 1 W
Number of RF Channels	EGSM: 124 DCS1900: 374 PCS1900: 300
Channel Spacing	200 kHz
Number of TX Power Levels	GSM900 *: 15 DCS1900: 16 PCS1900: 16

Transmitter characteristics

Item	Values (E-GSM/GSM1800)
Type	Direct conversion, nonlinear, FDMA/TDMA
LO frequency range	3520...3660 MHz / 3420...3570 MHz
Output power	2 W / 1 W peak
Gain control range	min. 30 dB
Maximum phase error (RMS/peak)	max 5 deg./20 deg. peak

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Receiver characteristics

Item	Values, E-GSM/GSM1800
Type	Direct conversion, Linear, FDMA/TDMA
LO frequencies	3700...3840 MHz / 3610...3760 MHz
Typical 3 dB bandwidth	+/- 91 kHz
Sensitivity	min. - 102 dBm (GSM1800 norm.cond. only)
Total typical receiver voltage gain (from antenna to RX ADC)	86 dB
Receiver output level (RF level -95 dBm)	230 mVpp, single-ended I/Q signals to RX ADCs
Typical AGC dynamic range	83 dB
Accurate AGC control range	60 dB
Typical AGC step in LNA	30 dB GSM1800 25 dB EGSM
Usable input dynamic range	-102... -10 dBm
RSSI dynamic range	-110... -48 dBm
Compensated gain variation in receiving band	+/- 1.0 dB

RF Block Diagram

The block diagram of the RF module can be seen in Chapter on “RF Block Diagram”. The detailed functional description is given in the following sections

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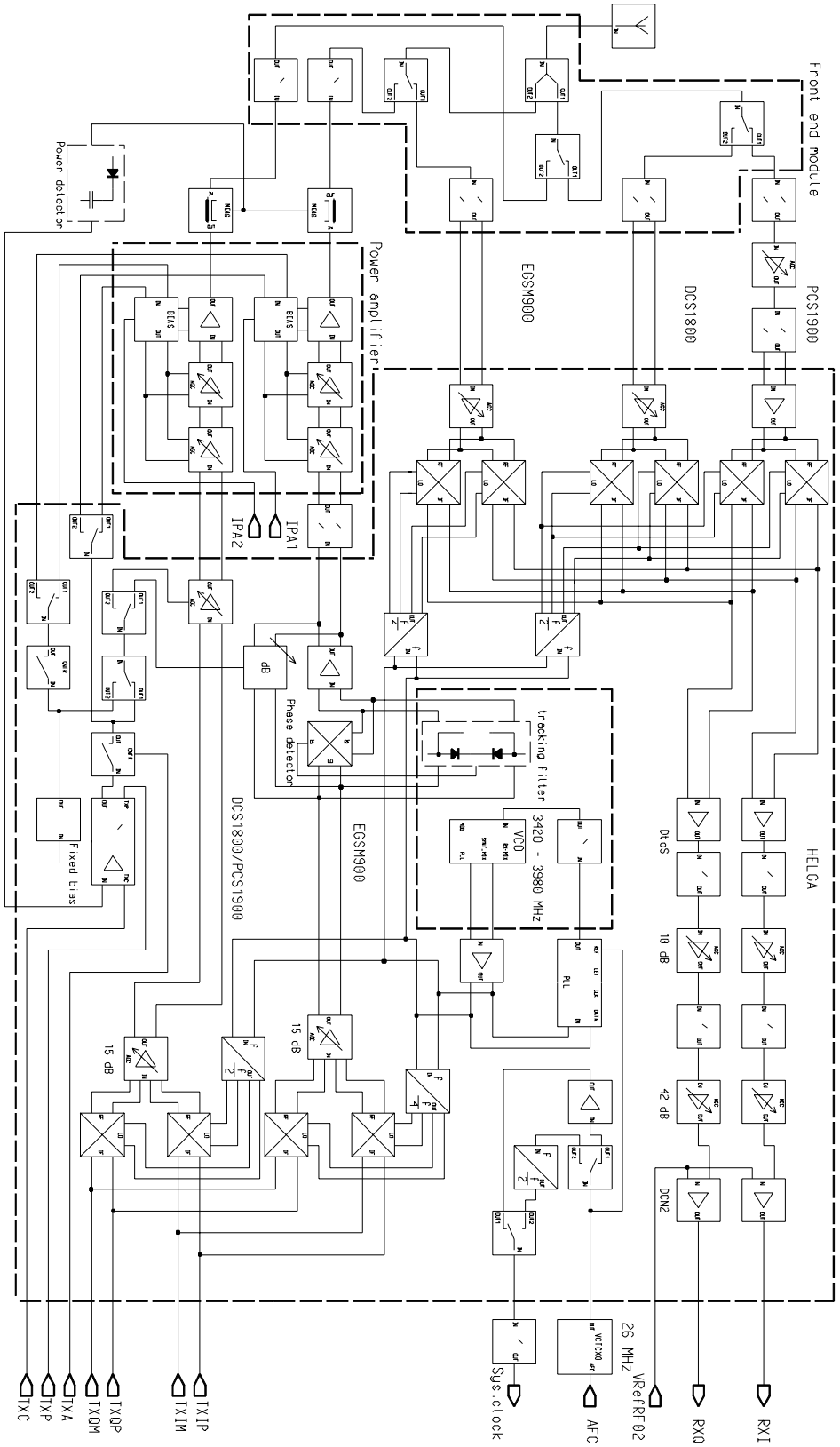
RF Block Diagram NHL-4J/NHL-4JX

Figure 21: RF Block Diagram



Frequency Synthesizers

The VCO frequency is locked by a PLL (phase locked loop) into a stable frequency source given by a VCTCXO which is running at 26 MHz. The frequency of the VCTCXO is in turn locked into the frequency of the base station with the help of an AFC voltage which is generated in UEM by an 11 bit D/A converter. The PLL is located in Helga and it is controlled through the RFBus.

The required frequency dividers for modulator and demodulator mixers are integrated in Helga.

Loop filter filters out the comparison pulses of the phase detector and generates a DC control voltage to the VCO. The loop filter determines the step response of the PLL (settling time) and contributes to the stability of the loop.

The frequency synthesizer is integrated in Helga except for the VCTCXO, VCO, and the loop filter.

Receiver

Each receiver path is a direct conversion linear receiver. From the antenna the received RF-signal is fed to a front end module where a diplexer first divides the signal to two separate paths according to the band of operation: either lower, EGSM900 or upper, DCS1800/PCS1900 path.

Most of the receiver circuitry is included in Helga.

Transmitter

The transmitter consists of two final frequency IQ-modulators and power amplifiers, for the lower and upper bands separately, and a power control loop. The IQ-modulators are integrated in Helga, as well as the operational amplifiers of the power control loop. The two power amplifiers are located in a single module and the power detector, directional coupler, and loop filter parts of the power control loop are implemented as discrete components on the PWB. In the GMSK mode the power is controlled by adjusting the DC bias levels of the power amplifiers.

Front End

The front end features include:

- Antenna 50 ohm input

- RX PCS single output, RX EGSM/DCS balanced output

- TXs single 50 ohm input

-3 control lines from the Helga

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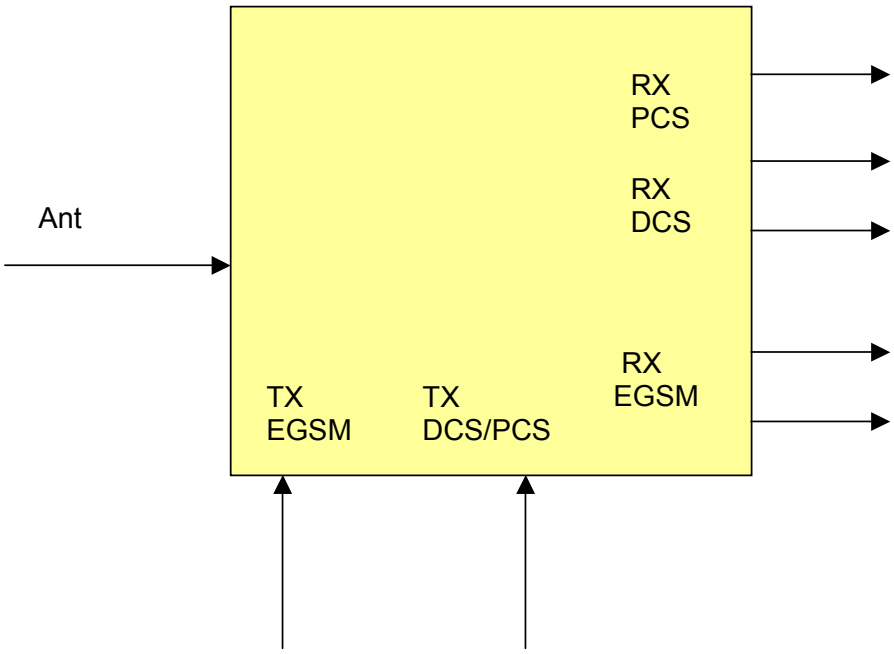
Figure 22: Front End



Power Amplifier

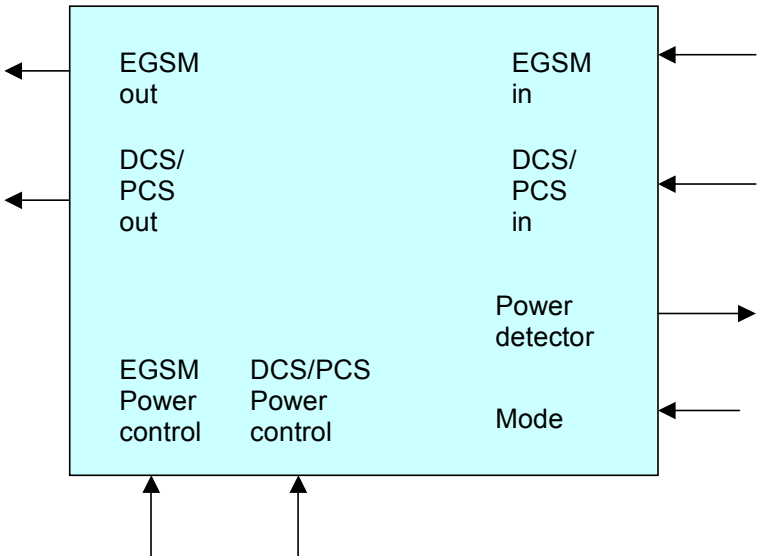
The power amplifier features include:

- 50 ohm input and output, EGSM/DCS/PCS

- internal power detector

- low power (EGSM) and EDGE mode

Figure 23: Power amplifier



RF ASIC Helga

The RF ASIC features include

- Package uBGA108

- Balanced I/Q demodulator and balanced I/Q modulator

- Power control operational amplifier, acts as an error amplifier

- The signal from VCO is balanced, frequencies 3420 to 3980 MHz

- EGSM and DCS low noise amplifier (LNA) are integrated.

The Helga can be tested by test points only.

AFC function

AFC is used to lock the transceiver's clock to the frequency of the base station.

Antenna

The NHL-4J/NHL-4JX GSM900/DCS1800/PCS1900 transceiver features an internal antenna.

User Interface Modules

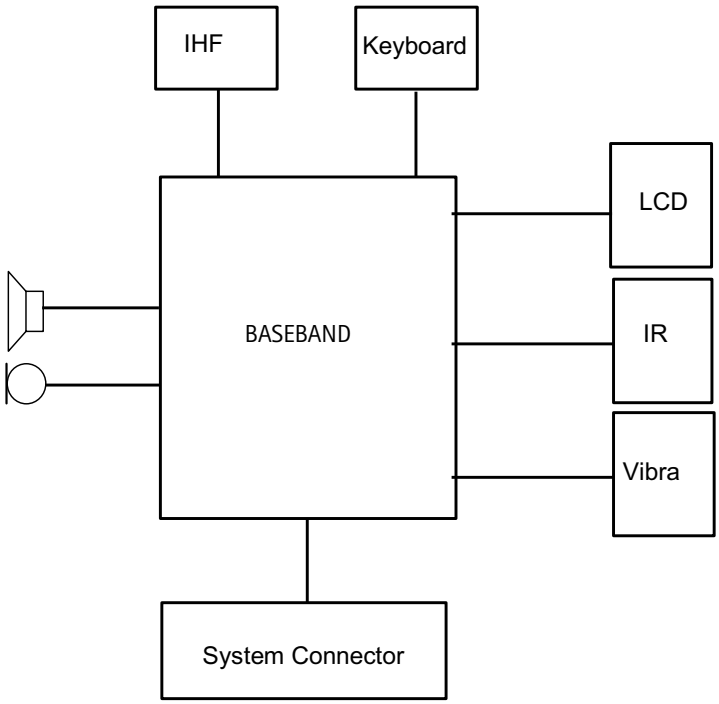
UI module consist of a separate 4-layer UI PWB TK8 for NHL-4J/NHL-4JX/4U.

The User Interface features a 130 x 130 8bpp (bits per pixel) passive matrix color STN display, 4096 colours. Interface is using 9-bit data transfer.

The LCD display is connected to transceiver PWB by board-to-board connector.

The diagram below describes the user interface connections.

Figure 24:



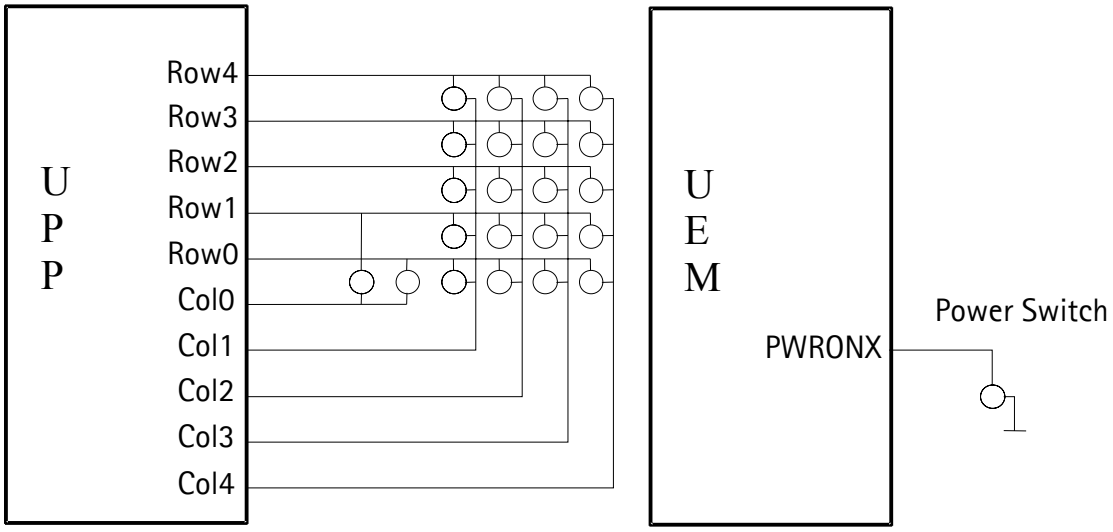
UI Board TK8

TK8 includes contacts for the keypad domes and LEDs for keypad illumination. UI board is connected to main PWB through 16 pole board-to-board connector with springs. Signals of the connector are described in External and Internal Signals and Connections.

Keyboard

5x4 matrix keyboard is used in NHL-4J/NHL-4JX. Key pressing is detected by scanning procedure. Keypad signals are connected UPP keyboard interface.

Figure 25:



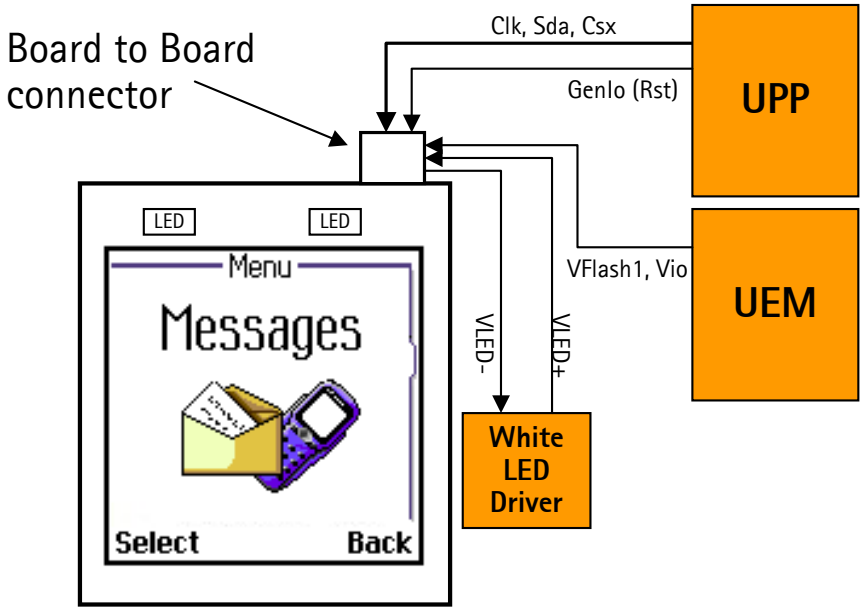
When no key is pressed row inputs are high due to UPP internal pull-up resistors. The columns are written zero. When key is pressed one row is pulled down and an interrupt is generated to MCU. After receiving inte rupt MCU starts scanning procedure. All columns are first written high and then one column at the time is written down. All other columns except one which was written down are set as inputs.

Rows are read while column at the time is written down. If some row is down it indicates that key which is at the cross point of selected column and row was pressed. After detect ing pressed key all register inside the UPP are reset and columns are written back to zero.

Display

The phone display is colour LCD.

Figure 26: LCD



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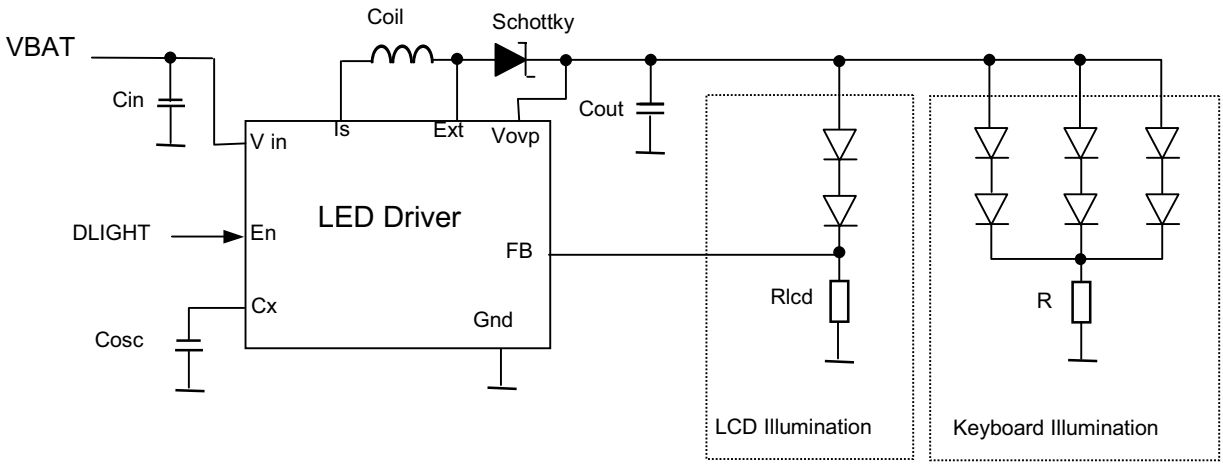
LCD & Keypad Illumination

In NHL-4J/NHL-4JX white leds are used for LCD and keypad illumination. For LCD illumination two leds are used and for keypad six leds.

Figure 27:



Current through leds is controlled by transistor circuitry. External transis tor driver circuitry is used as constant current source in order to prevent any change in battery voltage be seen as changing led brightness.

LEDs are controlled by the UEM PWM outputs. Both LEDs are controlled by *KLight* output of the UEM. Current flow through the LEDS is set by biasing the transistor and limiting the current by resistors.

Internal Speaker

The internal earpiece is a dynamic earpiece with an impedance of 32 ohms. The earpiece is low impedance one since the sound pressure is to be generated using current and not voltage as the supply voltage is re stricted to 2.7V. The earpiece is driven directly by the UEM and the ear piece driver in UEM is a bridge amplifier.

Buzzer

Buzzer is used to generate alerting tones and melodies to indicate incom ing call. It is also used to generate keypress and warning tones for the user. Buzzer is controlled by PWM (Pulse Width Modulation) signal generated by the buzzer driver of the UEM. Target SPL is 100dB (A) at 5cm.

Vibra

A vibra alerting device is used to generate a vibration signal for an incoming call. Vibra is located in the bottom end of the phone and connection is done with spring contacts. Vibra interface is the same like other DCT4 projects. The vibra is controlled by a PWM signal from the UEM. Frequency can be set to 64, 129, 258 or 520 Hz and duty cycle can vary between 3% - 97%.

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